FullFlex™ Synchronous DDR Dual-Port SRAM

Features

- **True dual-ported memory allows simultaneous access to the shared array from each port**
- **Synchronous pipelined operation with selectable Double Data Rate (DDR) or Single Data Rate (SDR) operation on each port**
  - **— DDR interface at 200 MHz**
  - **— SDR interface at 250 MHz**
  - **— Up to 36-Gb/s bandwidth (250 MHz * 72 bit * 2 ports)**
- **Selectable pipelined or flow-through mode**
- **1.5V or 1.8V core power supply**
- **Commercial and Industrial temperature ranges**
- **IEEE 1149.1 JTAG boundary scan**
- **Available in 484-ball PBGA Packages and 256-ball FBGA Packages**
- **FullFlex72 family**
  - **— 18 Mbit: 256K x 36 x 2 DDR or 256K x 72 SDR (CYDD18S72V18)**
  - **— 9 Mbit: 128K x 36 x 2 DDR or 128K x 72 SDR (CYDD09S72V18)**
  - **— 4 Mbit: 64K x 36 x 2 DDR or 64 x 72 SDR (CYDD04S72V18)**
- **FullFlex36 family**
  - **— 36 Mbit: 512K x 36 x 2 DDR (CYDD36S36V18)**
  - **— 18 Mbit: 256K x 36 x 2 DDR (CYDD18S36V18)**
  - **— 9 Mbit: 128K x 36 x 2 DDR (CYDD09S36V18)**
  - **— 4 Mbit: 64K x 36 x 2 DDR (CYDD04S36V18)**
- **FullFlex18 family**
  - **— 36 Mbit: 1M x 18 x 2 DDR (CYDD36S18V18)**
  - **— 18 Mbit: 512K x 18 x 2 DDR (CYDD18S18V18)**
  - **— 9 Mbit: 256K x 18 x 2 DDR (CYDD09S18V18)**
  - **— 4 Mbit: 128K x 18 x 2 DDR (CYDD04S18V18)**
- **Built-in deterministic access control to manage address collisions**
  - **— Deterministic flag output upon collision detection**
  - **— Collision detection on back-to-back clock cycles**
  - **— First Busy Address readback**
- **Advanced features for improved high-speed data transfer and flexibility**
  - **— Variable Impedance Matching (VIM)**
  - **— Echo clocks**
  - **— Selectable LVTTL (3.3V), Extended HSTL (1.4V–1.9V), 1.8V LVCMOS, or 2.5V LVCMOS I/O on each port**
  - **— Burst counters for sequential memory access**
  - **— Mailbox with interrupt flags for message passing**
  - **— Dual Chip Enables for easy depth expansion**

Functional Description

The FullFlex™ Dual-Port SRAM families consist of 4-Mbit, 9-Mbit, 18-Mbit, and 36-Mbit synchronous, true dual-port static RAMs that are high-speed, low-power 1.8V/1.5V CMOS. Two ports are provided, allowing the array to be accessed simultaneously. Simultaneous access to a location triggers deterministic access control. For FullFlex72, these ports can operate independently in DDR mode with 36-bit bus widths or in SDR mode with 72-bit bus widths. For FullFlex36 and FullFlex18, the ports operate in DDR mode only. Each port can be independently configured for two pipelined stages for SDR mode or 2.5 stages in DDR mode. Each port can also be configured to operate in pipelined or flow-through mode in SDR mode.

Advanced features include built-in deterministic access control to manage address collisions during simultaneous access to the same memory location, Variable Impedance Matching (VIM) to improve data transmission by matching the output driver impedance to the line impedance, and echo clocks to improve data transfer.

To reduce the static power consumption, chip enables can be used to power down the internal circuitry. The number of cycles of latency before a change in $\overline{CE0}$ or CE1 will enable or disable the databus matches the number of cycles of read latency selected for the device. In order for a valid write or read to occur, both chip enable inputs on a port must be active.

Each port contains an optional burst counter on the input address register. After externally loading the counter with the initial address, the counter will increment the address internally.

Additional features of this device include a mask register and a mirror register to control counter increments and wrap-around. The counter-interrupt ($\overline{CNTINT}$) flags notify the host that the counter will reach maximum count value on the next clock cycle. The host can read the burst-counter internal address, mask register address, and busy address on the address lines. The host can also load the counter with the address stored in the mirror register by utilizing the retransmit functionality. Mailbox interrupt flags can be used for message passing, and JTAG boundary scan and asynchronous Master Reset ($\overline{MRST}$) are also available. The logic block diagram in *Figure 1* displays these features.

The FullFlex72 DDR family of devices is offered in a 484-ball plastic BGA package. The FullFlex36 and FullFlex18 DDR only families of devices are offered in both 484-ball and 256-ball fine pitch BGA packages.

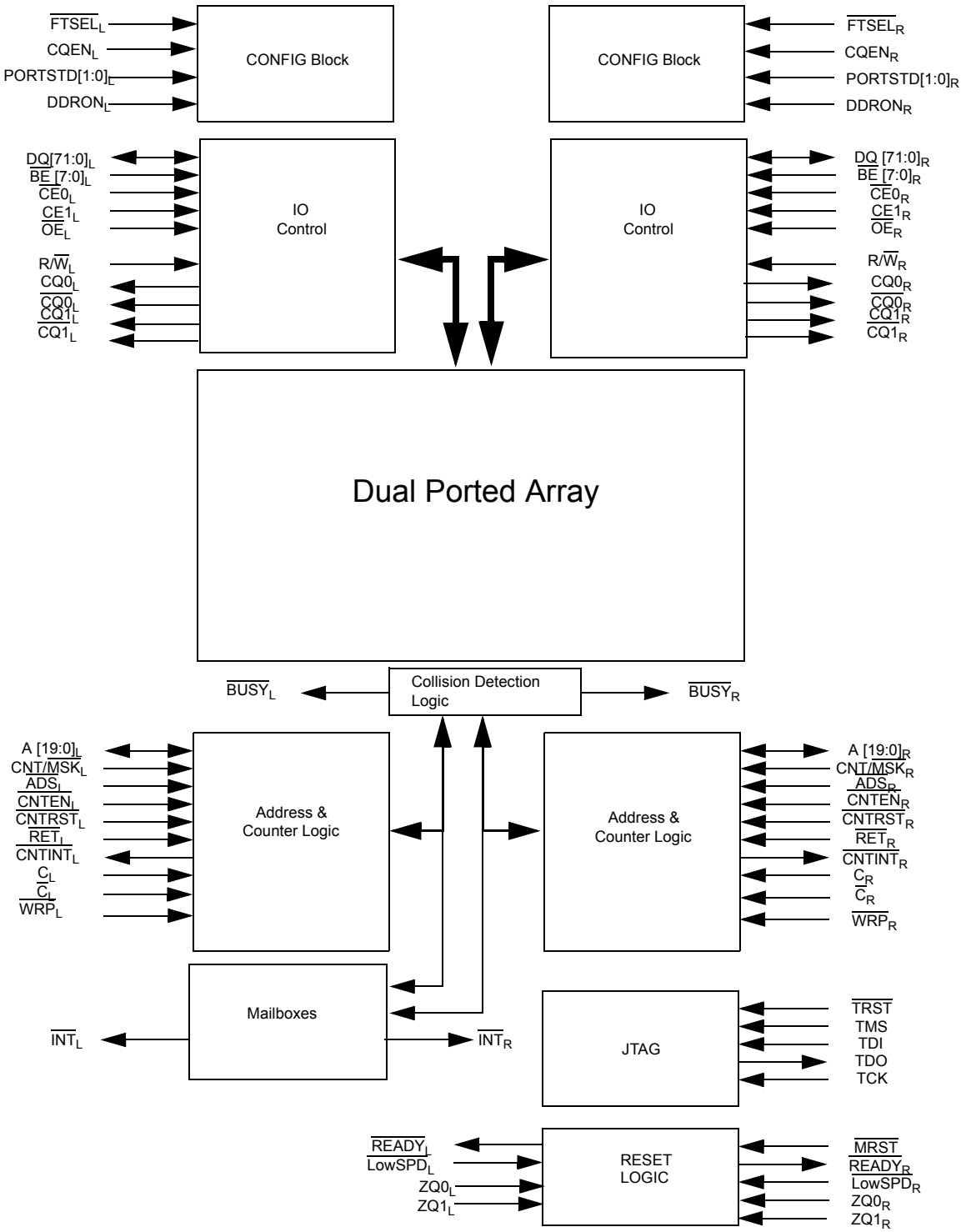


Figure 1. Block Diagram[1,2,3]

Notes:
1. The CYDD36S18V18 device has 20 address bits. The CYDD36S36V18, and the CYDD18S18V18 devices have 19 address bits. The CYDD18S72V18, CYDD18S36V18, and the CYDD09S18V18 devices have 18 address bits. The CYDD09S72V18, CYDD04S18V18, and the CYDD09S36V18 devices have 17 address bits. The CYDD04S36V18 and the CYDD04S72V18 devices have 16 address bits.
2. The FullFlex72 family of devices has 72 data lines. The FullFlex36 family of devices has 36 data lines. The FullFlex18 family of devices has 18 data lines.
3. The FullFlex72 family of devices has eight byte enables. The FullFlex36 family of devices has four byte enables. The FullFlex18 family of devices has two byte enables.

FullFlex72 SDR/DDR 484-ball BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DQ34L	DQ32L	DQ30L	DQ27L	DQ60L	DQ57L	DQ54L	DQ24L	DQ21L	DQ18L	DQ18R	DQ21R	DQ24R	DQ54R	DQ57R	DQ60R	DQ27R	DQ30R	DQ32R	DQ34R	DNU
B	DQ63L	DQ35L	DQ33L	DQ31L	DQ28L	DQ61L	DQ58L	DQ55L	DQ25L	DQ22L	DQ19L	DQ19R	DQ22R	DQ25R	DQ55R	DQ58R	DQ61R	DQ28R	DQ31R	DQ33R	DQ35R	DQ63R
C	DQ65L	DQ64L	VSS	VSS	DQ29L	DQ62L	DQ59L	DQ56L	DQ26L	DQ23L	DQ20L	DQ20R	DQ23R	DQ26R	DQ56R	DQ59R	DQ62R	DQ29R	VSS	VSS	DQ64R	DQ65R
D	DQ67L	DQ66L	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	DDRONL	$\overline{LOW}$/SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$L	$\overline{CNTI}$NTL	PORTSTD1L	DNU	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	DQ66R	DQ67R
E	DQ69L	DQ68L	VDDIOL	VSS	VSS	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	DNU	VSS	VDDIOR	DQ68R	DQ69R
F	DQ71L	DQ70L	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	DQ70R	DQ71R
G	A0L	A1L	$\overline{RETL}$	$\overline{BE2L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE2R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRP}$L	$\overline{BE6L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE6R}$	$\overline{WRP}$R	A3R	A2R
J	A4L	A5L	$\overline{READ}$YL	$\overline{BE3L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE3R}$	$\overline{READ}$YR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	$\overline{BE7L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	$\overline{BE7R}$	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	$\overline{CL}$	$\overline{BE5L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE5R}$	$\overline{CR}$	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	$\overline{BE1L}$	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE1R}$	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	CNT/$\overline{MSKL}$	$\overline{BE4L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE4R}$	CNT/$\overline{MSK}$R	A15R	A14R
R	A16L[7]	A17L[6]	$\overline{CNTE}$NL	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTE}$NR	A17R[6]	A16R[7]
T	A18L[5]	DNU	$\overline{CNTR}$STL	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTR}$STR	DNU	A18R[5]
U	DQ53L	DQ52L	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	DQ52R	DQ53R
V	DQ51L	DQ50L	$\overline{FTSE}$LL	VDDIOL	DNU	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{TRST}$	VDDIOR	$\overline{FTSE}$LR	DQ50R	DQ51R
W	DQ49L	DQ48L	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	DNU	PORTSTD1R	$\overline{CNTI}$NTR	$\overline{BUSY}$R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$/SPDR	DDRONR	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	DQ48R	DQ49R
Y	DQ47L	DQ46L	VSS	VSS	DQ11L	DQ44L	DQ41L	DQ38L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ38R	DQ41R	DQ44R	DQ11R	TMS	TCK	DQ46R	DQ47R
AA	DQ45L	DQ17L	DQ15L	DQ13L	DQ10L	DQ43L	DQ40L	DQ37L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ37R	DQ40R	DQ43R	DQ10R	DQ13R	DQ15R	DQ17R	DQ45R
AB	DNU	DQ16L	DQ14L	DQ12L	DQ9L	DQ42L	DQ39L	DQ36L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ36R	DQ39R	DQ42R	DQ9R	DQ12R	DQ14R	DQ16R	DNU

Notes:
4. Leaving this pin DNU disables VIM
5. Leave this ball unconnected for CYDD18S72V18, CYDD09S72V18 and CYDD04S72V18.
6. Leave this ball unconnected for CYDD09S72V18 and CYDD04S72V18
7. Leave this ball unconnected for CYDD04S72V18

FullFlex36 DDR 484-ball BGA Pinout (Top View)[8]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DNU	DNU	DNU	DNU	DQ33L	DQ30L	DQ27L	DQ24L	DQ21L	DQ18L	DQ18R	DQ21R	DQ24R	DQ27R	DQ30R	DQ33R	DNU	DNU	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DNU	DQ34L	DQ31L	DQ28L	DQ25L	DQ22L	DQ19L	DQ19R	DQ22R	DQ25R	DQ28R	DQ31R	DQ34R	DNU	DNU	DNU	DNU	DNU
C	DNU	DNU	VSS	VSS	DNU	DQ35L	DQ32L	DQ29L	DQ26L	DQ23L	DQ20L	DQ20R	DQ23R	DQ26R	DQ29R	DQ32R	DQ35R	DNU	VSS	VSS	DNU	DNU
D	DNU	DNU	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VDDIOL	$\overline{LOW}$ SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$ L	$\overline{CNTI}$ NTL	PORTSTD1L	DNU	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	DNU	DNU
E	DNU	DNU	VDDIOL	VSS	VSS	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	DNU	VSS	VDDIOR	DNU	DNU
F	DNU	DNU	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	DNU	DNU
G	A0L	A1L	$\overline{RETL}$	$\overline{BE2L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE2R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRP}$ L	$\overline{BE3L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE3R}$	$\overline{WRP}$ R	A3R	A2R
J	A4L	A5L	$\overline{READ}$ YL	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	$\overline{READ}$ YR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	DNU	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	$\overline{CL}$	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	$\overline{CR}$	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	DNU	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	CNT/MSKL	$\overline{BE1L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE1R}$	CNT/MSKR	A15R	A14R
R	A16L	A17L	$\overline{CNTE}$ NL	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTE}$ NR	A17R	A16R
T	A18L	DNU	$\overline{CNTR}$ STL	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTR}$ STR	DNU	A18R
U	DNU	DNU	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	DNU	DNU
V	DNU	DNU	VDDIOL	VDDIOL	DNU	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOR	$\overline{TRST}$	VDDIOR	VDDIOR	DNU	DNU
W	DNU	DNU	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	DNU	PORTSTD1R	$\overline{CNTI}$ NTR	$\overline{BUSY}$ R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$ SPDR	VDDIOR	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	DNU	DNU
Y	DNU	DNU	VSS	VSS	DNU	DQ17L	DQ14L	DQ11L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ11R	DQ14R	DQ17R	DNU	TMS	TCK	DNU	DNU
AA	DNU	DNU	DNU	DNU	DNU	DQ16L	DQ13L	DQ10L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ10R	DQ13R	DQ16R	DNU	DNU	DNU	DNU	DNU
AB	DNU	DNU	DNU	DNU	DNU	DQ15L	DQ12L	DQ9L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ9R	DQ12R	DQ15R	DNU	DNU	DNU	DNU	DNU

Note:
8. Use this pinout only for device CYDD36S36V18 of the FullFlex36 family.

FullFlex18 DDR 484-ball BGA Pinout (Top View)[9]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ15L	DQ12L	DQ9L	DQ9R	DQ12R	DQ15R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ16L	DQ13L	DQ10L	DQ10R	DQ13R	DQ16R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
C	DNU	DNU	VSS	VSS	DNU	DNU	DNU	DNU	DQ17L	DQ14L	DQ11L	DQ11R	DQ14R	DQ17R	DNU	DNU	DNU	DNU	VSS	VSS	DNU	DNU
D	DNU	DNU	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VDDIOL	$\overline{LOW}$/SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$L	$\overline{CNTI}$NTL	PORTSTD1L	DNU	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	DNU	DNU
E	DNU	DNU	VDDIOL	VSS	VSS	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	DNU	VSS	VDDIOR	DNU	DNU
F	DNU	DNU	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	DNU	DNU
G	A0L	A1L	$\overline{RETL}$	$\overline{BE1L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE1R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRP}$L	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	$\overline{WRP}$R	A3R	A2R
J	A4L	A5L	$\overline{READ}$YL	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	$\overline{READ}$YR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	DNU	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	$\overline{CL}$	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	$\overline{CR}$	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	DNU	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	CNT/$\overline{MSKL}$	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	CNT/$\overline{MSK}$R	A15R	A14R
R	A16L	A17L	$\overline{CNTE}$NL	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTE}$NR	A17R	A16R
T	A18L	A19L	$\overline{CNTR}$STL	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTR}$STR	A19R	A18R
U	DNU	DNU	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	DNU	DNU
V	DNU	DNU	VDDIOL	VDDIOL	DNU	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOR	$\overline{TRST}$	VDDIOR	VDDIOR	DNU	DNU
W	DNU	DNU	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	DNU	PORTSTD1R	$\overline{CNTI}$NTR	$\overline{BUSY}$R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$/SPDR	VDDIOR	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	DNU	DNU
Y	DNU	DNU	VSS	VSS	DNU	DNU	DNU	DNU	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DNU	DNU	DNU	DNU	TMS	TCK	DNU	DNU
AA	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
AB	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU

Note:
9. Use this pinout only for device CYDD36S18V18 of the FullFlex18 family.

FullFlex36 DDR 256 Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DQ32L	DQ30L	DQ28L	DQ26L	DQ24L	DQ22L	DQ20L	DQ18L	DQ18R	DQ20R	DQ22R	DQ24R	DQ26R	DQ28R	DQ30R	DQ32R
B	DQ33L	DQ31L	DQ29L	DQ27L	DQ25L	DQ23L	DQ21L	DQ19L	DQ19R	DQ21R	DQ23R	DQ25R	DQ27R	DQ29R	DQ31R	DQ33R
C	DQ34L	DQ35L	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	DNU	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	DQ35R	DQ34R
D	A0L	A1L	$\overline{\text{WRPL}}$	VREFL	VDDIOL	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	VDDIOR	VREFR	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNTINTL}}$	$\overline{\text{BE3L}}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE3R}}$	$\overline{\text{CNTINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	$\overline{\text{BE2L}}$	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE2R}}$	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	$\overline{\text{CL}}$	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	$\overline{\text{CR}}$	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L[11]	A17L[10]	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R[10]	A16R[11]
N	DNU	DNU	$\overline{\text{CNT/MSKL}}$	VREFL	PORTSTD0L	$\overline{\text{READYL}}$	ZQ1L[4]	VTTL	VTTL	ZQ1R[4]	$\overline{\text{READYR}}$	PORTSTD0R	VREFR	$\overline{\text{CNT/MSKR}}$	DNU	DNU
P	DQ16L	DQ17L	$\overline{\text{CNTENL}}$	$\overline{\text{CNTRSTL}}$	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	DQ17R	DQ16R
R	DQ15L	DQ13L	DQ11L	DQ9L	DQ7L	DQ5L	DQ3L	DQ1L	DQ1R	DQ3R	DQ5R	DQ7R	DQ9R	DQ11R	DQ13R	DQ15R
T	DQ14L	DQ12L	DQ10L	DQ8L	DQ6L	DQ4L	DQ2L	DQ0L	DQ0R	DQ2R	DQ4R	DQ6R	DQ8R	DQ10R	DQ12R	DQ14R

Notes:
10. Leave this ball unconnected for CYDD09S36V18 and CYDD04S36V18.
11. Leave this ball unconnected for CYDD04S36V18.

FullFlex18 DDR 256 Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DNU	DNU	DNU	DQ17L	DQ16L	DQ13L	DQ12L	DQ9L	DQ9R	DQ12R	DQ13R	DQ16R	DQ17R	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DQ15L	DQ14L	DQ11L	DQ10L	DQ10R	DQ11R	DQ14R	DQ15R	DNU	DNU	DNU	DNU
C	DNU	DNU	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	DNU	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	DNU	DNU
D	A0L	A1L	$\overline{\text{WRPL}}$	VREFL	VDDIOL	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	VDDIOR	VREFR	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNTINTL}}$	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VDDIOR	DNU	$\overline{\text{CNTINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	DNU	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	DNU	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	$\overline{\text{CL}}$	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	$\overline{\text{CR}}$	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L	A17L[13]	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R[13]	A16R
N	A18L[12]	DNU	CNT/$\overline{\text{MSKL}}$	VREFL	PORTSTD0L	$\overline{\text{READYL}}$	ZQ1L[4]	VTTL	VTTL	ZQ1R[4]	$\overline{\text{READYR}}$	PORTSTD0R	VREFR	CNT/$\overline{\text{MSKR}}$	DNU	A18R[12]
P	DNU	DNU	$\overline{\text{CNTENL}}$	$\overline{\text{CNTRSTL}}$	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	DNU	DNU
R	DNU	DNU	DNU	DNU	DQ6L	DQ5L	DQ2L	DQ1L	DQ1R	DQ2R	DQ5R	DQ6R	DNU	DNU	DNU	DNU
T	DNU	DNU	DNU	DQ8L	DQ7L	DQ4L	DQ3L	DQ0L	DQ0R	DQ3R	DQ4R	DQ7R	DQ8R	DNU	DNU	DNU

Table 1. Selection Guide

	–200	–167	Unit
SDR f_{MAX}[14]	250	200	MHz
DDR f_{MAX}[15]	200	167	MHz
SDR Max. Access Time (Clock to Data)	2.64	3.3	ns
DDR Max. Access Time (Clock to Data)	0.50	0.60	ns
Typical Operating Current I_{CC}	800[16]	700[16]	mA
Typical Standby Current for I_{SB3} (Both Ports CMOS Level)	210[16]]	210[16]	mA

Notes:
12. Leave this ball unconnected for CYDD09S18V18 and CYDD04S18V18.
13. Leave this ball unconnected for CYDD04S18V18.
14. SDR mode with two pipelined stages.
15. DDR mode with 2.5 pipelined stages.
16. For 18-Mbit x36x2 DDR commercial configuration only, please refer to the electrical characteristics section for complete information.

Pin Definitions

Left Port	Right Port	Description
$A[19:0]_L$	$A[19:0]_R$	**Address Inputs**.[1]
$DQ[71:0]_L$	$DQ[71:0]_R$	**Data Bus Input/Output**.[2]
$\overline{BE}[7:0]_L$	$\overline{BE}[7:0]_R$	**Byte Select Inputs**.[3] Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	**Port Busy Output**. When there is an address match and both chip enables are active for both ports, an external BUSY signal is asserted on the fifth clock cycle from when the collision occurs.
$C/\overline{C}_L$	$C/\overline{C}_R$	**Clock Signal**.[18] Maximum clock input rate is f_{MAX}. Tie $\overline{C}$ to VSS when operating in SDR mode.
$\overline{CE0}_L$	$\overline{CE0}_R$	**Active LOW Chip Enable Input.**
$CE1_L$	$CE1_R$	**Active HIGH Chip Enable Input**.
$CQEN_L$	$CQEN_R$	**Echo Clock Enable Input**. Assert HIGH to enable echo clocking on respective port.
$CQ0_L$	$CQ0_R$	**Echo Clock Signal Output for DQ[35:0] for FullFlex72 devices**. Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$\overline{CQ0}_L$	$\overline{CQ0}_R$	**Inverted Echo Clock Signal Output for DQ[35:0] for FullFlex72 devices**. Inverted Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$CQ1_L$	$CQ1_R$	**Echo Clock Signal Output for DQ[71:36] for FullFlex72 devices**. Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Echo Clock Signal Output for DQ[17:9] for FullFlex18 devices.
$\overline{CQ1}_L$	$\overline{CQ1}_R$	**Inverted Echo Clock Signal Output for DQ[71:36] for FullFlex72 devices**. Inverted Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[17:9] forFullFlex18 devices.
$DDRON_L$[17]	$DDRON_R$[17]	**DDR Enable Input**. Assert HIGH to enable DDR clocking on respective port.
$ZQ[1:0]_L$	$ZQ[1:0]_R$	**VIM Output Impedance Matching Input**. To use, connect a calibrating resistor between ZQ and ground. The resistor must be five times larger than the intended line impedance driven by the dual-port. Assert HIGH or leave DNU to disable Variable Impedance Matching.
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}_L$	$\overline{INT}_R$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{LowSPD}_L$	$\overline{LowSPD}_R$	**Port Low Speed Select Input**. Assert this pin LOW to disable the DLL. For operation at less than 100 MHz, assert this pin LOW.
$PORTSTD[1:0]_L$[19]	$PORTSTD[1:0]_R$[19]	**Port Clock/Address/Control/Data/Echo Clock/I/O Standard Select Input**. Assert these pins LOW/LOW for LVTTL, LOW/HIGH for HSTL, HIGH/LOW for 2.5V LVCMOS, and HIGH/HIGH for 1.8V LVCMOS, respectively. These pins must be driven by VTTL referenced levels.
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable Input**. Assert this pin LOW to Write to, or HIGH to Read from the dual-port memory array.
$\overline{READY}_L$	$\overline{READY}_R$	**Port DLL Ready Output**. This signal will be asserted LOW when the DLL and Variable Impedance Matching circuits have completed calibration. This is a wired OR capable output.
$CNT/\overline{MSK}_L$	$CNT/\overline{MSK}_R$	**Port Counter/Mask Select Input**. Counter control input.
$\overline{ADS}_L$	$\overline{ADS}_R$	**Port Counter Address Load Strobe Input**. Counter control input.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	**Port Counter Enable Input**. Counter control input.

Notes:
17. $DDRON_L$ and $DDRON_R$ needs to tie to the same voltage level for FullFlex36 and FullFlex18 Family.
18. C and $\overline{C}$ are complimentary for DDR operation.
19. $PORTSTD[1:0]_L$ and $PORTSTD[1:0]_R$ have internal pull-down resistors.

Pin Definitions (continued)

Left Port	Right Port	Description
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	**Port Counter Reset Input**. Counter control input.
$\overline{CNTINT}_L$	$\overline{CNTINT}_R$	**Port Counter Interrupt Output**. This pin is asserted LOW one cycle before the unmasked portion of the counter is incremented to all “1s”.
$\overline{WRP}_L$	$\overline{WRP}_R$	**Port Counter Wrap Input**. When the burst counter reaches the maximum count, on the next counter increment WRP can be set LOW to load the unmasked counter bits to 0 or set HIGH to load the counter with the value stored in the mirror register.
$\overline{RET}_L$	$\overline{RET}_R$	**Port Counter Retransmit Input**. Assert this pin LOW to reload the initial address for repeated access to the same segment of memory.
$VREF_L$	$VREF_R$	**Port External HSTL I/O Reference Input**. This pin is left DNU when HSTL is not used.
$VDDIO_L$	$VDDIO_R$	**Port Data I/O Power Supply**.
$\overline{FTSEL}_L$	$\overline{FTSEL}_R$	**Port Flow-through Mode Select Input**. Assert this pin LOW to select Flow-through mode. Assert this pin HIGH to select Pipelined mode. Selection for SDR only.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting MRST LOW performs all of the reset functions as described in the text. A MRST operation is required at power-up. This pin must be driven by $VDDIO_L$ referenced levels.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. Operation for LVTTL or 2.5V LVCMOS.
TDI		**JTAG Test Data Input**. Data on the TDI input will be shifted serially into selected registers. Operation for LVTTL or 2.5V LVCMOS.
$\overline{TRST}$		**JTAG Reset Input**. Operation for LVTTL or 2.5V LVCMOS.
TCK		**JTAG Test Clock Input**. Operation for LVTTL or 2.5V LVCMOS.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP. Operation for LVTTL or 2.5V LVCMOS.
VSS		**Ground Inputs**.
VCORE		**Device Core Power Supply**.
VTTL		**LVTTL Power Supply**.

Selectable I/O Standard

The FullFlex device families also offer the option of choosing one of four port standards for the device. Each port can independently select standards from single-ended HSTL class I, single-ended LVTTL, 2.5V LVCMOS, or 1.8V LVCMOS. The selection of the standard is determined by the PORTSTD pins for each port. These pins must be connected to a VTTL power supply. This will determine the input clock, address, control, data, and Echo clock standard for each port as shown in *Table 2*. Please note that only 1.8V LVCMOS and HSTL are supported for 4-Mbit, 9-Mbit, 18-Mbit devices running at 250MHz SDR, and for 36-Mbit devices running at 200 MHz SDR.

Table 2. Port Standard Selection

PORTSTD1	PORTSTD0	I/O Standard
VSS	VSS	LVTTL
VSS	VTTL	HSTL
VTTL	VSS	2.5V LVCMOS
VTTL	VTTL	1.8V LVCMOS

Clocking

Separate clocks synchronize the operations on each port. Each port has two clock inputs C and $\overline{C}$. In SDR mode only the C input clock is used and $\overline{C}$ should be tied to VSS. In this mode, all the transactions on the address, control, and data will be on the C rising edge. In DDR mode, both C and $\overline{C}$ will be used and these signals are complementary. In this mode, all transactions on the address and control, except for the byte enables, will occur on the C rising edge. Transactions on the data input, output, and byte enables will be on the C and $\overline{C}$ rising edges.

Double Data Rate (DDR)

In DDR mode with a x36 bus width, the input data is sampled on both edges of the input clock. During a write, on the rising edge of C, the first 36 bits (DQ[71:36]) will be latched into a register. On the rising edge of $\overline{C}$, the next 36 bits (DQ[35:0]) will be latched into a register. During a read, the first 36 bits are driven out first on the rising edge of C. The next 36 bits will be driven out on the rising edge of C. The internal bus width of the FullFlex72 family is still x72. All counter operation is based upon the x72 word width. The DDR option is set on a per port basis by the configuration of the DDRON pin. *Table 3* shows the data assignment for SDR and DDR configuration. The column on the right (Data Pin Name) shows the pins on which data is presented on the data lines.

Table 3. Data Pin Assignment for SDR and DDR Configuration

$\overline{BE}$ Pin Name for DDR	$\overline{BE}$ Pin Name for SDR	x72 SDR Mode	x36 DDR Mode		
		Data Pin Name	Related Rising Edge Clock for Write	Related Rising Edge Clock for Read	Data Pin Name
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[71]	C	$\overline{C}$	DQ[35]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[35]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[70]	C	$\overline{C}$	DQ[34]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[34]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[69]	C	$\overline{C}$	DQ[33]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[33]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[68]	C	$\overline{C}$	DQ[32]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[32]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[67]	C	$\overline{C}$	DQ[31]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[31]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[66]	C	$\overline{C}$	DQ[30]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[30]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[65]	C	$\overline{C}$	DQ[29]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[29]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[64]	C	$\overline{C}$	DQ[28]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[28]	$\overline{C}$	C	
$\overline{BE}$[3]	$\overline{BE}$[7]	DQ[63]	C	$\overline{C}$	DQ[27]
$\overline{BE}$[3]	$\overline{BE}$[3]	DQ[27]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[62]	C	$\overline{C}$	DQ[26]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[26]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[61]	C	$\overline{C}$	DQ[25]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[25]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[60]	C	$\overline{C}$	DQ[24]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[24]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[59]	C	$\overline{C}$	DQ[23]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[23]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[58]	C	$\overline{C}$	DQ[22]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[22]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[57]	C	$\overline{C}$	DQ[21]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[21]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[56]	C	$\overline{C}$	DQ[20]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[20]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[55]	C	$\overline{C}$	DQ[19]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[19]	$\overline{C}$	C	
$\overline{BE}$[2]	$\overline{BE}$[6]	DQ[54]	C	$\overline{C}$	DQ[18]
$\overline{BE}$[2]	$\overline{BE}$[2]	DQ[18]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[53]	C	$\overline{C}$	DQ[17]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[17]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[52]	C	$\overline{C}$	DQ[16]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[16]	$\overline{C}$	C	

Table 3. Data Pin Assignment for SDR and DDR Configuration (continued)

$\overline{BE}$ Pin Name for DDR	$\overline{BE}$ Pin Name for SDR	x72 SDR Mode	x36 DDR Mode		
		Data Pin Name	Related Rising Edge Clock for Write	Related Rising Edge Clock for Read	Data Pin Name
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[51]	C	$\overline{C}$	DQ[15]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[15]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[50]	C	$\overline{C}$	DQ[14]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[14]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[49]	C	$\overline{C}$	DQ[13]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[13]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[48]	C	$\overline{C}$	DQ[12]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[12]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[47]	C	$\overline{C}$	DQ[11]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[11]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[46]	C	$\overline{C}$	DQ[10]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[10]	$\overline{C}$	C	
$\overline{BE}$[1]	$\overline{BE}$[5]	DQ[45]	C	$\overline{C}$	DQ[9]
$\overline{BE}$[1]	$\overline{BE}$[1]	DQ[9]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[44]	C	$\overline{C}$	DQ[8]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[8]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[43]	C	$\overline{C}$	DQ[7]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[7]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[42]	C	$\overline{C}$	DQ[6]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[6]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[41]	C	$\overline{C}$	DQ[5]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[5]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[40]	C	$\overline{C}$	DQ[4]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[4]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[39]	C	$\overline{C}$	DQ[3]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[3]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[38]	C	$\overline{C}$	DQ[2]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[2]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[37]	C	$\overline{C}$	DQ[1]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[1]	$\overline{C}$	C	
$\overline{BE}$[0]	$\overline{BE}$[4]	DQ[36]	C	$\overline{C}$	DQ[0]
$\overline{BE}$[0]	$\overline{BE}$[0]	DQ[0]	$\overline{C}$	C	

Selectable Pipelined/Flow-through Mode

To meet data rate and throughput requirements, the FullFlex families offer selectable pipelined or flow-through mode. Flow-through mode is only supported in the FullFlex72 devices when the port is configured in SDR mode. Echo clocks are not supported in flow-through mode and the DLL must be disabled.

Flow-through mode is selected by the $\overline{FTSEL}$ pin. Strapping this pin HIGH selects pipelined mode. Strapping this pin LOW selects flow-through mode.

DLL

The FullFlex families of devices have an on-chip DLL. Enabling the DLL reduces the clock to data valid (t_{CD}) time allowing more setup time for the receiving device. For operation at or below 100 MHz, the DLL must be disabled. This is selectable by strapping LowSPD LOW.

Whenever the operating frequency is altered beyond the Clock Input Cycle to Cycle Jitter spec, the DLL is required to be reset followed by 1024 clocks before any valid operation.

$\overline{LowSPD}$ pins can be used to reset the DLL(s) for a single port independent of all other circuitry. $\overline{MRST}$ can be used to reset

all DLLs on the chip, for information on DLL lock and reset time, please see the Master Reset section below.

Echo Clocking

As the speed of data increases, on-board delays caused by parasitics make providing accurate clock trees extremely difficult. To counter this problem, the FullFlex families incorporate Echo Clocks. Echo Clocks are enabled on a per port basis. The dual-port receives input clocks (C and $\overline{C}$ for DDR mode, C for SDR mode) that are used to clock in the address and control signals for a read operation. The dual-port retransmits the input clocks relative to the data output. The buffered clocks are provided on the CQ1, $\overline{CQ1}$, CQ0, and $\overline{CQ0}$ outputs. Each port has two pairs of Echo clocks. Each clock is associated with half the data bits. The output clock will match the corresponding ports I/O configuration.

To enable Echo clock outputs, tie CQEN HIGH. To disable Echo clock outputs, tie CQEN LOW.

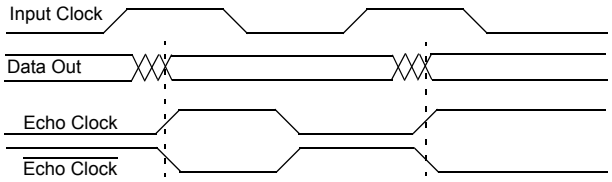


Figure 2. SDR Echo Clock Delay

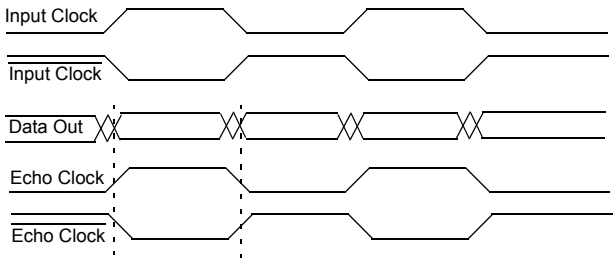


Figure 3. DDR Echo Clock Delay

Deterministic Access Control

Deterministic Access Control is provided for ease of design. The circuitry detects when both ports are accessing the same location and provides an external BUSY flag to the port on which data may be corrupted. The collision detection logic saves the address in conflict (Busy Address) to a readable register. In the case of multiple collisions, the first Busy address will be written to the Busy Address register.

If both ports are accessing the same location at the same time and only one port is doing a write, if t_{CCS} is met, then the data being written to and read from the address is valid data. For example, if the right port is reading and the left port is writing and the left ports clock meets t_{CCS}, then the data being read from the address by the right port will be the old data. In the same case, if the right ports clock meets t_{CCS}, then the data being read out of the address from the right port will be the new data. In the above case, if t_{CCS} is violated by the either ports clock with respect to the other port and the right port gets the external $\overline{BUSY}$ flag, the data from the right port is corrupted. *Table 4* shows the t_{CCS} timing that must be met to guarantee the data.

Table 5 shows that in the case of the left port writing and the right port reading, when an external $\overline{BUSY}$ flag is asserted on the right port, the data read out of the device will not be guaranteed.

The value in the busy address register can be read back to the address lines. The required input control signals for this function are shown in *Table 8*. The value in the busy address register will be read out to the address lines t_{CA} after the same amount of latency as a data read operation in SDR mode. In DDR mode, the address latency is only 2 cycles instead of 2.5 which is the data latency. After an initial address match, the address under contention is saved in the busy address register. All following address matches cause the $\overline{BUSY}$ flag to be generated, however, none of the addresses are saved into the busy address register. Once a busy readback is performed, the address of the first match which happens at least two clock cycles after the busy readback is saved into the busy address register.

Table 4. t_{CCS} Timing for All Operating Modes

Port A – Early Arriving Port		Port B – Late Arriving Port		t_{CCS} C/$\overline{C}$ Rise to Opposite C/$\overline{C}$ Rise Set-up Time for Non-corrupt Data	Unit
Mode	Active Edge	Mode	Active Edge		
SDR	C	SDR	C	$t_{CYC(min)} - 0.5$	ns
SDR	C	DDR	$\overline{C}$	$t_{CYC(min)} - 0.5$	ns
DDR	$\overline{C}$	SDR	C	$0.55 * t_{CYC} + t_{CYC(min)} - 1$	ns
DDR	$\overline{C}$	DDR	$\overline{C}$	$0.55 * t_{CYC} + t_{CYC(min)} - 1$	ns

Table 5. Deterministic Access Control Winning Port

Left Port	Right Port	Clock Timing		$\overline{BUSY}_L$	$\overline{BUSY}_R$	Description
		Left Clock	Right Clock			
Read	Read	X	X	H	H	No Collision
Write	Read	$>t_{CCS}$	0	H	H	Read OLD Data
		0	$>t_{CCS}$	H	H	Read NEW Data
		$<t_{CCS}$	0	H	H	Read OLD Data
				H	L	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read NEW Data
				H	L	Data Not Guaranteed
Read	Write	$>t_{CCS}$	0	H	H	Read NEW Data
		0	$>t_{CCS}$	H	H	Read OLD Data
		$<t_{CCS}$	0	H	H	Read NEW Data
				L	H	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read OLD Data
				L	H	Data Not Guaranteed
Write	Write	0	$>-t_{CCS}$ & $<t_{CCS}$	L	L	Array Data Corrupted
		0	$>t_{CCS}$	L	H	Array Stores Right Port Data
		$>t_{CCS}$	0	H	L	Array Stores Left Port Data

Variable Impedance Matching (VIM)

Each port contains a Variable Impedance Matching circuit to set the impedance of the I/O driver to match the impedance of the on-board traces. The impedance is set for all outputs except JTAG and is done on a per port basis. To take advantage of the VIM feature, connect a calibrating resistor (RQ) that is five times the value of the intended line impedance from the ZQ pin to VSS. The output impedance is then adjusted to account for drifts in supply voltage and temperature every 1024 clock cycles. If a port's clock is suspended, the VIM circuit will retain its last setting until the clock is restarted. On restart, it will then resume periodic adjustment. In the case of a significant change in device temperature or supply voltage, recalibration will happen every 1024 clock cycles. A Master Reset will initialize the VIM circuitry. *Table 6* shows the VIM parameters and *Table 7* describes the VIM operation modes.

In order to disable VIM, the ZQ pin must be connected to VDDIO of the relative supply for the I/Os before a Master Reset.

Table 6. Variable Impedance Matching Parameters

Parameter	Min.	Max.	Unit	Tolerance
RQ Value	100	275	Ω	±2%
Output Impedance	20	55	Ω	±15%
Reset Time	N/A	1024	Cycles	N/A
Update Time	N/A	1024	Cycles	N/A

Table 7. Variable Impedance Matching Operation

RQ Connection	Output Configuration
100Ω–275Ω to VSS	Output Driver Impedance = RQ/5 ± 15% at Vout = VDDIO/2
ZQ to VDDIO	VIM Disabled. Rout ≤ 20Ω at Vout = VDDIO/2

Address Counter and Mask Register Operations[1]

Each port of the FullFlex families contains a programmable burst address counter. The burst counter contains four registers: a counter register, a mask register, a mirror register, and a busy address register.

The **counter register** contains the address used to access the RAM array. It is changed only by the master reset ($\overline{MRST}$), Counter Reset, Counter Load, Retransmit, and Counter Increment operations.

The **mask register** value affects the Counter Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is only changed by Mask Reset, Mask Load, and MRST. The Mask Load operation loads the value of the address bus into the mask register. The mask register defines the counting range of the counter register. The mask register is divided into two or three consecutive regions. Zero or more “0s” define the masked region and one or more “1s” define the unmasked portion of the counter register. The counter register may only be divided into up to three regions. The region containing the least significant bits must be no more than two “0s”. Bits one and zero may be “10” respectively, masking the least significant counter bit and causing the counter to increment by two instead of one. If bits one and zero are “00”, the two least significant bits are masked and the counter will increment by four instead of one. For example, in the case of a 256Kx72 configuration, a mask register value of 003FC divides the mask register into three regions. With bit 0 being the least significant bit and bit 17 being the most significant bit, the two least significant bits are masked, the next eight bits are unmasked, and the remaining bits are masked.

The **mirror register** is used to reload the counter register on retransmit operations (see “retransmit” below) and wrap functions (see “counter increment” below). The last value loaded into the counter register is stored in the mirror register. The mirror register is only changed by master reset (MRST), Counter Reset, and Counter Load.

Table 8 summarizes the operations of these registers and the required input control signals. All signals except MRST are synchronized to the ports clock.

Counter Load Operation[1]

The address counter and mirror registers are both loaded with the address value presented on the address lines. This value ranges from 0 to FFFFF.

Mask Load Operation[1]

The mask register is loaded with the address value presented on the address bus. This value ranges from 0 to FFFFF though not all values permit correct increment operations. Permitted values are in the form of 2^n–1, 2^n–2, or 2^n–4. The counter register can only be segmented in up to three regions. From the most significant bit to the least significant bit, permitted values have zero or more “0s”, one or more “1s”, and the least significant two bits can be “11”, “10”, or “00”. Thus FFFFE, 7FFFF, and 03FFC are permitted values but 2FFFF, 03FFA, and 7FFE4 are not.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. The address will be valid t_{CA} after the selected number of latency cycles configured by FTSEL. This is the same as data in SDR mode and one half cycle earlier than data latency for DDR mode. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. *Figure 4* shows a block diagram of the logic.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. The address will be valid t_{CA} after the selected number of latency cycles configured by FTSEL. For pipelined SDR and DDR mode this is two cycles. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. *Figure 4* shows a block diagram of the operation.

Table 8. Burst Counter and Mask Register Control Operation (Any Port) [20,21]

C	MRST	CNTRST	CNT/MSK	CNTEN	ADS	RET	Operation	Description
X	L	X	X	X	X	X	Master Reset	Reset address counter to all 0s, mask register to all 1s, and busy address to all 0’s.
⎍	H	L	H	X	X	X	Counter Reset	Reset counter and mirror unmasked portion to all 0s.
⎍	H	L	L	X	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	H	H	L	L	X	Counter Load	Load burst counter and mirror with external address value presented on address lines.
⎍	H	H	L	L	L	X	Mask Load	Load mask register with value presented on the address lines.
⎍	H	H	H	L	H	L	Retransmit	Load counter with value in the mirror register
⎍	H	H	H	L	H	H	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.

Notes:
20. X” = “Don’t Care”, “H” = HIGH, “L” = LOW.
21. Counter operation and mask register operation is independent of chip enables.

Table 8. Burst Counter and Mask Register Control Operation (Any Port) (continued)[20,21]

C	$\overline{MRST}$	$\overline{CNTRST}$	CNT/$\overline{MSK}$	$\overline{CNTEN}$	$\overline{ADS}$	$\overline{RET}$	Operation	Description
↑	H	H	L	H	H	L	Busy Address Readback	Read out first busy address after last busy address readback
↑	H	H	L	L	H	X	Reserved	
↑	H	H	L	H	L	L	Reserved	
↑	H	H	L	H	H	H	Reserved	
↑	H	H	H	H	L	L	Reserved	
↑	H	H	H	H	H	L	Reserved	

Counter Reset Operation

All unmasked bits of the counter are reset to “0”. All masked bits remain unchanged. The new burst counter value is loaded into the mirror registers. A mask reset followed by a counter reset will reset the counter and mirror registers to 00000.

Mask Reset Operation

The mask register is reset to all “1s”, which unmasks every bit of the burst counter.

Increment Operation[1]

Once the address counter is initially loaded with an external address, the counter can internally increment the address value and address the entire memory array. Only the unmasked bits of the counter register are incremented. In order for a counter bit to change, the corresponding bit in the mask register must be “1”. If the two least significant bits of the mask register are “11”, the burst counter will increment by one. If the two least significant bits are “10”, the burst counter will increment by two, and if they are “00”, the burst counter will increment by four. If all unmasked counter bits are incremented to “1” and $\overline{WRP}$ is deasserted, the next increment will wrap the counter back to the initially loaded value. The cycle before the increment that results in all unmasked counter bits to become “1s”, a counter interrupt flag ($\overline{CNTINT}$) is asserted if the counter is incremented again. This increment will cause the counter to reach its maximum value and the next increment will return the counter register to its initial value that was stored in the mirror register if $\overline{WRP}$ is deasserted. If $\overline{WRP}$ is asserted, the unmasked portion of the counter is filled with “0” instead. The example shown in *Figure 5* shows an example of the CYDD36S18V18 device with the mask register loaded with a mask value of 0007F unmasking the seven least significant bits. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 00005 assuming $\overline{WRP}$ is deasserted. The base address bits (in this case, the seventh address through the twentieth address) do not increment once the counter is configured for increment operation. The counter address will start at address 00005 and will increment its internal address value until it reaches the mask register value of 0007F. The counter wraps around the memory block to location 00005 at the next count. $\overline{CNTINT}$ is issued when the counter reaches the maximum –1 count.

Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Retransmit

Retransmit allows repeated access to the same block of memory without the need to reload the initial address. An internal mirror register stores the address counter value last loaded. While $\overline{RET}$ is asserted low, the counter will continue to wrap back to the value in the mirror register independent of the state of $\overline{WRP}$.

Counter Interrupt

The counter interrupt ($\overline{CNTINT}$) is asserted LOW one clock cycle before an increment operation that results in the unmasked portion of the counter register being all “1s”. It is deasserted by counter reset, counter load, mask reset, mask load, counter increment, re-transmit, and $\overline{MRST}$.

Counting by Two

When the two least significant bits of the mask register are “10,” the counter increments by two.

Counting by Four

When the two least significant bits of the mask register are “00,” the counter increments by four.

Mailbox Interrupts

The upper two memory locations can be used for message passing and permit communications between ports. *Table 9* shows the interrupt operation for both ports. The highest memory location is the mailbox for the right port and the maximum address–1 is the mailbox for the left port.

When one port Writes to the other ports mailbox, the $\overline{INT}$ flag of the port that the mailbox belongs to is asserted LOW. The $\overline{INT}$ flag remains asserted until the mailbox location is read by the other port. When a port reads it’s mailbox, the $\overline{INT}$ flag is deasserted HIGH after one cycle of latency with respect to the input clock of the port to which the mailbox belongs and is independent of $\overline{OE}$.

Table 9 shows that in order to set the $\overline{INT}_R$ flag, a Write operation by the left port to address FFFFF will assert $\overline{INT}_R$ LOW. A valid Read of the FFFFF location by the right port will reset $\overline{INT}_R$ HIGH after one cycle of latency with respect to the

right port's clock. At least one byte enable has to be activated to set or reset the mailbox interrupt.

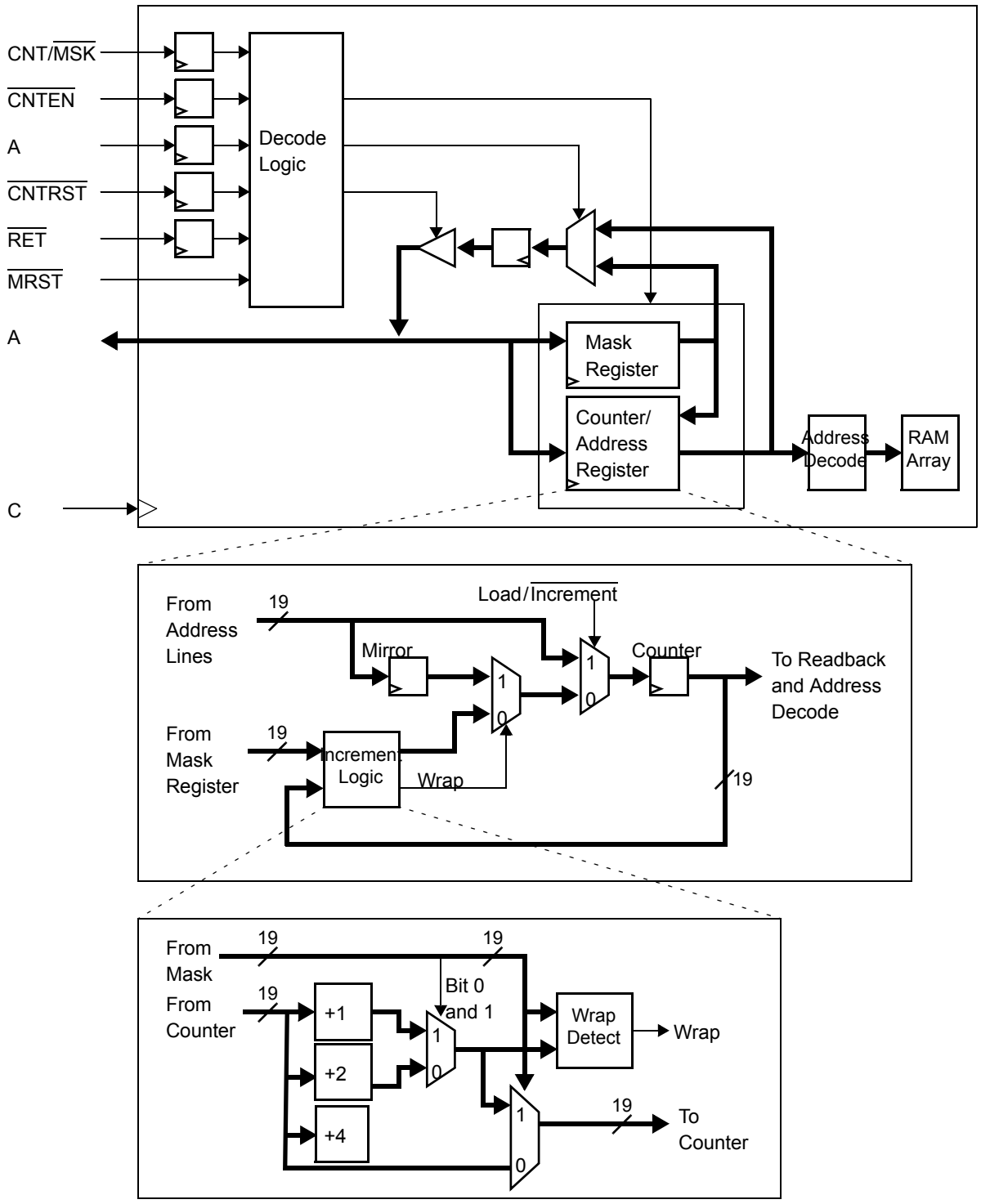


Figure 4. Counter, Mask, and Mirror Logic Block Diagram[1]

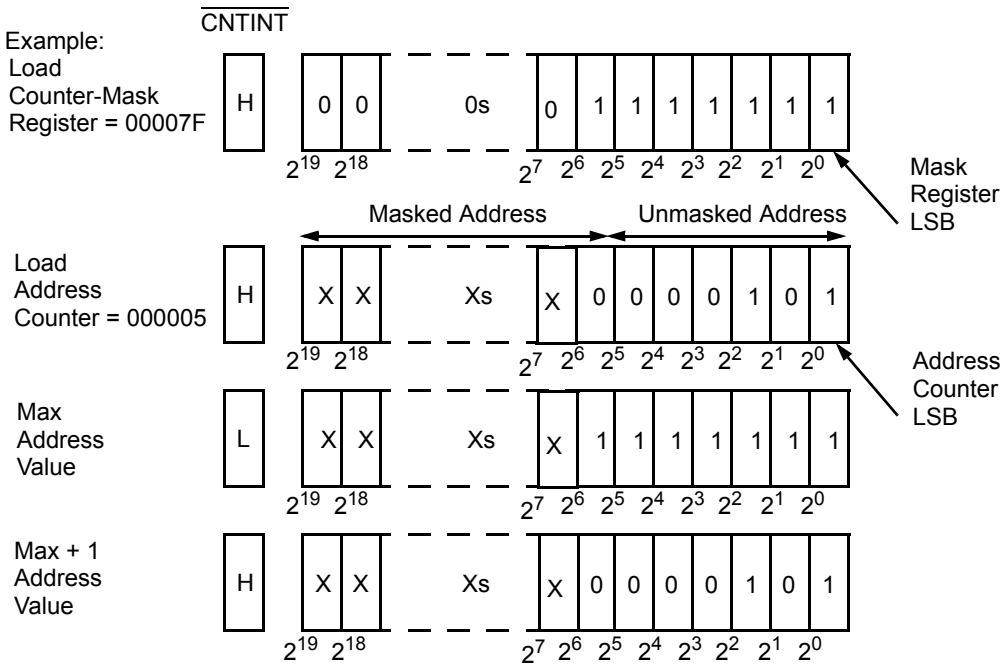


Figure 5. Programmable Counter-Mask Register Operation with $\overline{WRP}$ deasserted[1,25]

Table 9. Interrupt Operation Example [1, 20, 22, 23, 24]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	$A_{0L–19L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$A_{0R–19R}$	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	Max. Address	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	Max. Address	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	Max. Address–1	X
Reset Left $\overline{INT}_L$ Flag	H	L	Max. Address–1	H	X	X	X	X

Master Reset

The FullFlex family of dual-ports undergo a complete reset when MRST is asserted. MRST must be driven by $VDDIO_L$ referenced levels. The MRST can be asserted asynchronously to the clocks and must remain asserted for at least t_{RS}. Once asserted MRST deasserts READY, initializes the internal burst counters, internal mirror registers, and internal Busy Addresses to zero, and initializes the internal mask register to all “1s”. All mailbox interrupts (INT), Busy Address Outputs (BUSY), and burst counter interrupts (CNTINT) are deasserted upon master reset. Additionally, MRST must not be released until all power supplies including VREF are fully ramped, all port clocks and mode select inputs (LOWSPD, ZQ, CQEN, DDRON, FTSEL, and PORTSTD) are valid and stable. This begins calibration of the DLL and VIM circuits. READY will be asserted within 1024 clock cycles. READY is a wired OR capable output with a strong pull-up and weak pull-down. Up to four outputs may be connected together. For faster pull-down of the signal, connect a 250-Ω resistor to VSS. If the DLL and VIM circuits are disabled for a port, the port will be operational within five clock cycles. However, the READY will be asserted within 160 clock cycles.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The FullFlex families incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels depending on the VTTL power supply. It is composed of four input connections and one output connection required by the test logic defined by the standard.

Notes:
22. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, $\overline{CE}$ only needs to be asserted once at the rising edge of the C and can be deasserted after that. Data will be out after the following C edge and will be tri-stated after the next C edge.
23. $\overline{OE}$ is “Don’t Care” for mailbox operation.
24. At least one of $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, $\overline{BE3}$, $\overline{BE4}$, $\overline{BE5}$, $\overline{BE6}$, or $\overline{BE7}$ must be LOW.
25. The “X” in this diagram represents the counter’s upper bits.

Table 10.JTAG IDCODE Register Definitions

Part Number	Configuration	Value
CYDD36S36V18	512Kx72	0C041069h
CYDD36S18V18	1024Kx36	0C042069h
CYDD18S72V18	256Kx72	0C043069h
CYDD18S36V18	256Kx72	0C044069h
CYDD18S18V18	512Kx36	0C045069h
CYDD09S72V18	128Kx72	0C046069h
CYDD09S36V18	128Kx72	0C047069h
CYDD09S18V18	256Kx36	0C048069h
CYDD04S72V18	64Kx72	0C049069h
CYDD04S36V18	64Kx72	0C04A069h
CYDD04S18V18	128Kx36	0C04B069h

Table 11.Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[26]

Table 12.Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all FullFlex72 and FullFlex36 output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Note:
26. Details of the boundary scan length can be found in the BSDL file for the device.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to + 4.1V

DC Voltage Applied to Outputs in High-Z State.....–0.5V to V_{DDIO} + 0.5V

DC Input Voltage.....–0.5V to V_{DDIO} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage .....> 2200V

(JEDEC JESD8-6, JESD8-B)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	VCORE
Commercial	0°C to +70°C	1.8V ± 100 mV 1.5V ± 80 mV
Industrial	–40°C to +85°C	1.8V ± 100 mV 1.5V ± 80 mV

Power Supply Requirements

	Min.	Typ.	Max.
LVTTL VDDIO	3.0V	3.3V	3.6V
2.5V LVCMOS VDDIO	2.3V	2.5V	2.7V
HSTL VDDIO	1.4V	1.5V	1.9V
1.8V LVCMOS VDDIO	1.7V	1.8V	1.9V
3.3V VTTL	3.0V	3.3V	3.6V
2.5V VTTL	2.3V	2.5V	2.7V
HSTL VREF	0.68V	0.75V	0.95V

Electrical Characteristics Over the Operating Range

Parameter	Description	Configuration	All Speed Bins[27]			Unit
			Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{DDIO} = Min., I_{OH} = –8 mA)	LVTTL	2.4[28]			V
	(V_{DDIO} = Min., I_{OH} = –4 mA)	HSTL(DC)[29]	VDDIO – 0.4[28]			V
	(V_{DDIO}= Min., I_{OH} = –4 mA)	HSTL(AC)[29]	VDDIO – 0.5[28]			V
	(V_{DDIO} = Min., I_{OH} = –6 mA)	2.5V LVCMOS	1.7[28]			V
	(V_{DDIO} = Min., I_{OH} = –4 mA)	1.8V LVCMOS	VDDIO – 0.45[28]			V
V_{OL}	Output HIGH Voltage (V_{DDIO} = Min., I_{OL} = 8 mA)	LVTTL			0.4[28]	V
	(V_{DDIO} = Min., I_{OL} = 4 mA)	HSTL(DC)[29]			0.4[28]	V
	(V_{DDIO} = Min., I_{OL} = 4 mA)	HSTL(AC)[29]			0.5[28]	V
	(V_{DDIO} = Min., I_{OL} = 6 mA)	2.5V LVCMOS			0.7[28]	V
	(V_{DDIO} = Min., I_{OL} = 4 mA)	1.8V LVCMOS			0.45[28]	V
V_{IH}	Input HIGH Voltage	LVTTL	2		VDDIO + 0.3	V
		HSTL(DC)[29]	VREF + 0.1		VDDIO + 0.3	V
		2.5V LVCMOS	1.7			V
		1.8V LVCMOS	1.26			V
V_{IL}	Input LOW Voltage	LVTTL	–0.3		0.8	V
		HSTL(DC)[29]	–0.3		VREF – 0.1	V
		2.5V LVCMOS	0.7			V
		1.8V LVCMOS	0.36			V

Notes:
27. LVTTL and 2.5V LVCMOS are not available for 4-Mbit, 9-Mbit, 18-Mbit devices running at 250 MHz SDR and 36-Mbit devices running at 200 MHz SDR.
28. These parameters are met with VIM disabled.
29. The (DC) specifications are measured under steady state conditions. The (AC) specifications are measured while switching at speed. AC VIH/VIL in HSTL mode are measured with 1V/ns input edge rates

Electrical Characteristics Over the Operating Range (continued)

$\overline{READY}$ V_{OH}	Output HIGH Voltage (V_{DDIO} = Min., I_{OH} = –24 mA)	LVTTL	2.7[28]			V
	(V_{DDIO} = Min., I_{OH} = –12 mA)	HSTL(DC)[29]	VDDIO – 0.4[28]			V
	(V_{DDIO} = Min., I_{OH} = –12 mA)	HSTL(AC)[29]	VDDIO – 0.5[28]			V
	(V_{DDIO} = Min., I_{OH} = –15 mA)	2.5V LVCMOS	2.0[28]			V
	(V_{DDIO} = Min., I_{OH} = –12 mA)	1.8V LVCMOS	VDDIO – 0.45[28]			V
$\overline{READY}$ V_{OL}	Output HIGH Voltage (V_{DDIO} = Min., I_{OL} = 0.12 mA)	LVTTL			0.4[28]	V
	(V_{DDIO} = Min., I_{OL} = 0.12 mA)	HSTL(DC)[29]			0.4[28]	V
	(V_{DDIO} = Min., I_{OL} = 0.12 mA)	HSTL(AC)[29]			0.5[28]	V
	(V_{DDIO} = Min., I_{OL} = 0.15 mA)	2.5V LVCMOS			0.7[28]	V
	(V_{DDIO} = Min., I_{OL} = 0.08 mA)	1.8V LVCMOS			0.45[28]	V
I_{OZ}	Output Leakage Current		–10		10	µA
I_{IX1}	Input Leakage Current		–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, $\overline{MRST}$, $\overline{TRST}$, TCK		–300		10	µA
I_{IX3}	Input Leakage Current PORTSTD, DDRON		–10		300	µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Configuration		–200[27]		–167[27]		–133		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Operating Current (V_{CORE} = Max., I_{OUT} = 0 mA) Outputs Disabled	512Kx72 SDR[30]	Com.	N/A	N/A	1440	1800	1280	1620	mA
			Ind.	N/A	N/A	N/A	N/A	1330	1730	mA
		512Kx36x2 DDR	Com.	N/A	N/A	1280	1620	1120	1430	mA
			Ind.	N/A	N/A	N/A	N/A	1170	1550	mA
		1024Kx18x2 DDR	Com.	N/A	N/A	1050	1350	930	1220	mA
			Ind.	N/A	N/A	N/A	N/A	980	1330	mA
		256Kx72 SDR[30]	Com.	930	1140	800	980	N/A	N/A	mA
			Ind.	N/A	N/A	820	1030	N/A	N/A	mA
		256Kx36x2 DDR	Com.	800	980	700	880	N/A	N/A	mA
			Ind.	N/A	N/A	730	930	N/A	N/A	mA
		512Kx18x2 DDR	Com.	640	800	570	720	N/A	N/A	mA
			Ind.	N/A	N/A	590	780	N/A	N/A	mA
		128Kx72 SDR[30]	Com.	770	930	640	790	N/A	N/A	mA
			Ind.	N/A	N/A	660	830	N/A	N/A	mA
		128Kx36x2 DDR	Com.	640	790	560	700	N/A	N/A	mA
			Ind.	N/A	N/A	580	740	N/A	N/A	mA
		256Kx18x2 DDR	Com.	540	640	470	570	N/A	N/A	mA
			Ind.	N/A	N/A	490	600	N/A	N/A	mA
		64Kx72 SDR[30]	Com.	740	880	620	740	N/A	N/A	mA
			Ind.	N/A	N/A	630	770	N/A	N/A	mA
		64Kx36x2 DDR	Com.	620	740	540	650	N/A	N/A	mA
			Ind.	N/A	N/A	550	680	N/A	N/A	mA
		128Kx18x2 DDR	Com.	510	590	450	520	N/A	N/A	mA
			Ind.	N/A	N/A	460	530	N/A	N/A	mA

Note:
30. Use this number if any one of the two ports is operating in SDR mode.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration		–200[27]		–167[27]		–133		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	512Kx72 SDR[30]	Com.	N/A	N/A	1000	1250	920	1160	mA
			Ind.	N/A	N/A	N/A	N/A	970	1260	mA
		512Kx36x2 DDR	Com.	N/A	N/A	920	1160	830	1060	mA
			Ind.	N/A	N/A	N/A	N/A	880	1170	mA
		1024Kx18x2 DDR	Com.	N/A	N/A	820	1050	740	960	mA
			Ind.	N/A	N/A	N/A	N/A	790	1080	mA
		256Kx72 SDR[30]	Com.	570	700	500	630	N/A	N/A	mA
			Ind.	N/A	N/A	530	680	N/A	N/A	mA
		256Kx36x2 DDR	Com.	500	630	460	580	N/A	N/A	mA
			Ind.	N/A	N/A	490	630	N/A	N/A	mA
		512Kx18x2 DDR	Com.	460	570	410	530	N/A	N/A	mA
			Ind.	N/A	N/A	440	580	N/A	N/A	mA
		128Kx72 SDR[30]	Com.	460	560	400	490	N/A	N/A	mA
			Ind.	N/A	N/A	420	540	N/A	N/A	mA
		128Kx36x2 DDR	Com.	400	490	360	450	N/A	N/A	mA
			Ind.	N/A	N/A	380	490	N/A	N/A	mA
		256Kx18x2 DDR	Com.	380	440	340	400	N/A	N/A	mA
			Ind.	N/A	N/A	360	430	N/A	N/A	mA
		64Kx72 SDR[30]	Com.	440	520	380	450	N/A	N/A	mA
			Ind.	N/A	N/A	390	480	N/A	N/A	mA
		64Kx36x2 DDR	Com.	380	450	340	400	N/A	N/A	mA
			Ind.	N/A	N/A	350	430	N/A	N/A	mA
		128Kx18x2 DDR	Com.	360	400	320	360	N/A	N/A	mA
			Ind.	N/A	N/A	330	370	N/A	N/A	mA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration		–200[27]		–167[27]		–133		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{SB2}	Standby Current (One Port TTL or CMOS Level) $\overline{CE_L}$ | $\overline{CE_R} \geq V_{IH}$, $f = f_{MAX}$	512Kx72 SDR[30]	Com.	N/A	N/A	1300	1570	1160	1410	mA
			Ind.	N/A	N/A	N/A	N/A	1210	1520	mA
		512Kx36x2 DDR	Com.	N/A	N/A	1160	1410	1020	1260	mA
			Ind.	N/A	N/A	N/A	N/A	1070	1370	mA
		1024Kx18x2 DDR	Com.	N/A	N/A	980	1210	870	1100	mA
			Ind.	N/A	N/A	N/A	N/A	920	1210	mA
		256Kx72 SDR[30]	Com.	760	890	650	790	N/A	N/A	mA
			Ind.	N/A	N/A	680	840	N/A	N/A	mA
		256Kx36x2 DDR	Com.	650	790	580	710	N/A	N/A	mA
			Ind.	N/A	N/A	610	760	N/A	N/A	mA
		512Kx18x2 DDR	Com.	550	670	490	610	N/A	N/A	mA
			Ind.	N/A	N/A	520	670	N/A	N/A	mA
		128Kx72 SDR[30]	Com.	620	730	520	630	N/A	N/A	mA
			Ind.	N/A	N/A	550	670	N/A	N/A	mA
		128Kx36x2 DDR	Com.	520	630	460	560	N/A	N/A	mA
			Ind.	N/A	N/A	480	610	N/A	N/A	mA
		256Kx18x2 DDR	Com.	460	530	400	470	N/A	N/A	mA
			Ind.	N/A	N/A	430	500	N/A	N/A	mA
		64Kx72 SDR[30]	Com.	590	680	500	580	N/A	N/A	mA
			Ind.	N/A	N/A	510	610	N/A	N/A	mA
		64Kx36x2 DDR	Com.	500	580	440	510	N/A	N/A	mA
			Ind.	N/A	N/A	450	550	N/A	N/A	mA
		128Kx18x2 DDR	Com.	440	480	380	420	N/A	N/A	mA
			Ind.	N/A	N/A	390	440	N/A	N/A	mA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration		All Speed Bins[27] Typ.	All Speed Bins[27] Max.	Unit
I_{SB3}	Standby Current (Both Ports CMOS Level) CE_L and $CE_R \geq V_{CORE} - 0.2V$, f = 0	512Kx72 SDR[30]	Com.	410	590	mA
			Ind.	460	700	mA
		512Kx36x2 DDR	Com.	410	590	mA
			Ind.	460	700	mA
		1024Kx18x2 DDR	Com.	410	590	mA
			Ind.	460	700	mA
		256Kx72 SDR[30]	Com.	210	300	mA
			Ind.	230	350	mA
		256Kx36x2 DDR	Com.	210	300	mA
			Ind.	230	350	mA
		512Kx18x2 DDR	Com.	210	300	mA
			Ind.	230	350	mA
		128Kx72 SDR[30]	Com.	150	200	mA
			Ind.	170	220	mA
		128Kx36x2 DDR	Com.	150	200	mA
			Ind.	170	220	mA
		256Kx18x2 DDR	Com.	150	200	mA
			Ind.	170	220	mA
		64Kx72 SDR[30]	Com.	130	150	mA
			Ind.	140	170	mA
		64Kx36x2 DDR	Com.	130	150	mA
			Ind.	140	170	mA
		128Kx18x2 DDR	Com.	130	150	mA
			Ind.	140	170	mA

Table 13.Capacitance

Signals	Packages			
	CYDD18S72V18 CYDD09S72V18 CYDD04S72V18 CYDD18S36V18 CYDD09S36V18 CYDD04S36V18	CYDD18S18V18 CYDD09S18V18 CYDD04S18V18	CYDD36S36V18	CYDD36S18V18
$\overline{OE}$	12 pF	12 pF	20 pF	20 pF
$\overline{BE}$, DQ	10 pF	18 pF	16 pF	30 pF
All other signals	10 pF	10 pF	16 pF	16 pF

AC Test Load and Waveforms

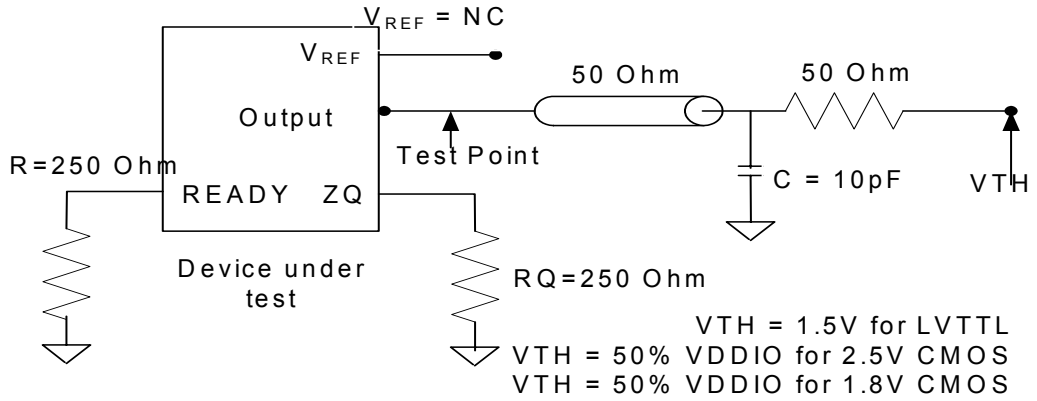


Figure 6. Output Test Load for LVTTL/CMOS

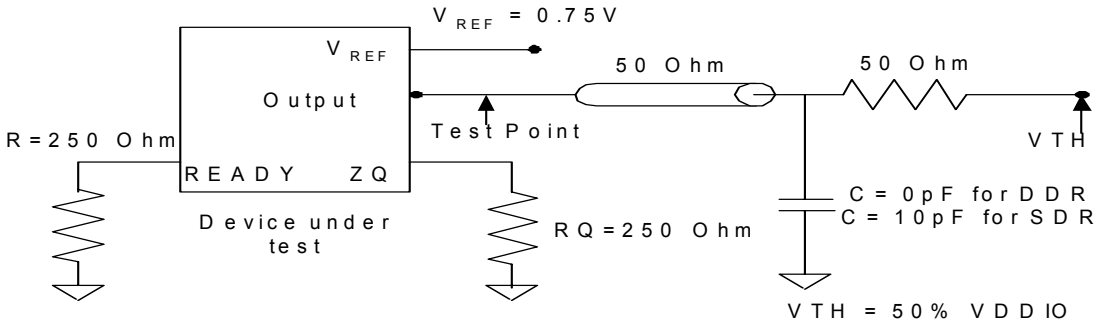
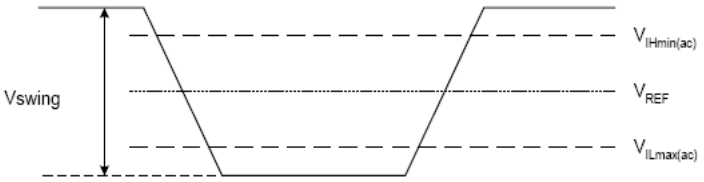


Figure 7. Output Test Load for HSTL

AC Input Test Signal Waveform



Vswing = 1.0V
VREF = 0.75V
V_{IH}= 1.25V
V_{IL} = 0.25V
Slew = 2.0V/ns
All input parameters are referenced to VREF

Figure 8. HSTL Input Waveform

Switching Characteristics Over the Operating Range

Table 14.DDR Mode with 2.5 Pipelined Stages and DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[33]

Parameter	Description		–200		–167		–133		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Operating Frequency		159	200	127	167	100	133	MHz
t_{CYC}	C/$\overline{C}$ Clock Cycle Time		5.00[34]	6.3	6.00[34]	7.88	7.50[34]	10.00	ns
t_{CH}	C/$\overline{C}$ Clock HIGH Time		2.00		2.40		3.00		ns
t_{CL}	C/$\overline{C}$ Clock LOW Time		2.00		2.40		3.00		ns
t_{CHCH}	C/$\overline{C}$ Clock Rise to $\overline{C}$/C Clock Rise		2.20		2.70		3.38		ns
t_{SD}	Data Input Set-up Time to C/$\overline{C}$ Rise	HSTL 1.8V LVCMOS	0.45[32]		0.55[32]		0.75[32]		ns
		2.5V LVCMOS 3.3V LVTTL	0.65[32]		0.75[32]		0.95[32]		ns
t_{HD}	Data Input Hold Time after C/$\overline{C}$ Rise		0.45		0.55		0.75		ns
t_{SBE}	Byte enable Set-up Time to C/$\overline{C}$ Rise	HSTL 1.8V LVCMOS	0.45[32]		0.55[32,]		0.65[32]		ns
		2.5V LVCMOS 3.3V LVTTL	0.65[32]		0.75[32]		0.85[32]		ns
t_{HBE}	Byte enable Hold Time after C/$\overline{C}$ Rise		0.45		0.55		0.65		ns
t_{SAC}	Address & Control Input except $\overline{BE}$ Set-up Time to C Rise	HSTL 1.8V LVCMOS	1.50[34]		1.70[34]		1.80[34]		ns
		2.5V LVCMOS 3.3V LVTTL	1.75[34]		1.95[34]		2.05[34]		ns
t_{HAC}	Address & Control Input except $\overline{BE}$ Hold Time after C Rise		0.50		0.60		0.70		ns
t_{OE}	Output Enable to Data Valid			4.40[32,34]		5.00[32,34]		5.50[32,34]	ns
t_{OLZ}[31]	$\overline{OE}$ to Low Z		1.00		1.00		1.00		ns
t_{OHZ}[31]	$\overline{OE}$ to High Z		1.00	4.40[32,34]	1.00	5.00[32,34]	1.00	5.50[32,34]	ns
t_{CD}[35]	C/$\overline{C}$ Rise to DQ Valid	HSTL 1.8V LVCMOS		0.65[32]		0.75[32]		0.85[32]	ns
		2.5V LVCMOS 3.3V LVTTL		0.65[32]		0.75[32]		0.85[32]	ns
t_{DC}[35]	DQ Output Hold after C/$\overline{C}$ Rise	HSTL 1.8V LVCMOS	–0.65		–0.75		–0.85		ns
		2.5V LVCMOS 3.3V LVTTL	–0.65		–0.75		–0.85		ns
t_{CCQ}[35]	C/$\overline{C}$ Rise to CQ/$\overline{CQ}$ Rise	HSTL 1.8V LVCMOS	–0.65[36]	0.65	–0.75[36]	0.75	–0.85[36]	0.85	ns
		2.5V LVCMOS 3.3V LVTTL	–0.65[36]	0.60	–0.75[36]	0.70	–0.85[36]	0.80	ns
t_{CQHQV}[35]	Echo Clock (CQ/$\overline{CQ}$) High to Output Valid	HSTL 1.8V LVCMOS		0.35[32]		0.40[32]		0.50[32]	ns
		2.5V LVCMOS 3.3V LVTTL		0.45[32]		0.50[32]		0.60[32]	ns

Notes:
31. Parameters specified with the load capacitance in *Figure 6* and *Figure 7*.
32. For the x18 devices, add 200 ps to this parameter in the table above.
33. Test conditions assume a signal transition time of 2 V/ns.
34. Add 15% to this parameter if a VCORE of 1.5V is used.
35. This parameter assumes input clock cycle to cycle jitter of +/- 0ps.
36. For the x18 devices, subtract 200ps from this parameter in the table above.

Table 14.DDR Mode with 2.5 Pipelined Stages and DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[33]

Parameter	Description		–200 Min.	–200 Max.	–167 Min.	–167 Max.	–133 Min.	–133 Max.	Unit
t_{CQHQX}[35]	Echo Clock (CQ/$\overline{CQ}$) High to Output Hold	HSTL 1.8V LVCMOS	–0.35[36]		–0.40[36]		–0.50[36]		ns
		2.5V LVCMOS 3.3V LVTTL	–0.50[36]		–0.55[36]		–0.65[36]		ns
t_{CKHZ}[31,35]	$\overline{C}$ Rise to DQ Output High Z	HSTL 1.8V LVCMOS		0.65[32]		0.75[32]		0.85[32]	ns
		2.5V LVCMOS 3.3V LVTTL		0.65[32]		0.75[32]		0.85[32]	ns
t_{CKLZ}[31,35]	$\overline{C}$ Rise to DQ Output Low Z	HSTL 1.8V LVCMOS	–0.65		–0.75		–0.85		ns
		2.5V LVCMOS 3.3V LVTTL	–0.65		–0.75		–0.85		ns
t_{CA}	C Rise to Address Readback Valid			5.00[34]		6.00[34]		7.50[34]	ns
t_{AC}	Address Output Hold after C Rise		1.00		1.00		1.00		ns
t_{CKHZA}[31]	C Rise to Address Output High Z		1.00	5.00[34]	1.00	6.00[34]	1.00	7.50[34]	ns
t_{CKLZA}[31]	C Rise to Address Output Low Z		1.00		1.00		1.00		ns
t_{SCINT}	C Rise to $\overline{\text{CNTINT}}$ Low		1.00	3.30[34]	1.00	4.00[34]	1.00	5.00[34]	ns
t_{RCINT}	C Rise to $\overline{\text{CNTINT}}$ High		1.00	3.30[34]	1.00	4.00[34]	1.00	5.00[34]	ns
t_{SINT}	$\overline{C}$ Rise to $\overline{\text{INT}}$ Low		0.50	7.00[34]	0.50	8.00[34]	0.50	9.00[34]	ns
t_{RINT}	$\overline{C}$ Rise to $\overline{\text{INT}}$ High		0.50	7.00[34]	0.50	8.00[34]	0.50	9.00[34]	ns
t_{BSY}	C Rise to $\overline{\text{BUSY}}$ Valid		1.00	3.30[34]	1.00	4.00[34]	1.00	5.00[34]	ns
t_{JIT}	Clock Input Cycle to Cycle Jitter			+/- 200		+/- 200		+/- 200	ps

Table 15.SDR Mode with Flow-Through Mode

Parameter	Description	–200[27] Min.	–200[27] Max.	–167[27] Min.	–167[27] Max.	–133 Min.	–133 Max.	Unit
f_{MAX} (FLOW-THROUGH)	Maximum Operating Frequency for Flow-through Mode		100		77		66.7	MHz
t_{CYC} (FLOW-THROUGH)	C Clock Cycle Time for Flow-through mode	10.00[34]		13.00[34]		15.00[34]		ns
t_{CD1}	C Rise to DQ Valid for Flow-through Mode (LowSPD = 1)		7.20[32,34]		9.00[32,34]		11.00[32, 34]	ns
t_{CA1}	C Rise to Address Readback Valid for Flow-through Mode		7.20[34]		9.00[34]		11.00[34]	ns
t_{CKHZ1}[31]	C Rise to DQ Output High Z in Flow-through Mode	1.00	7.20[32,34]	1.00	9.00[32,34]	1.00	11.00[32, 34]	ns
t_{CKLZ1}[31]	C Rise to DQ Output Low Z in Flow-through Mode	1.00		1.00		1.00		ns
t_{CKHZA1}[31]	C Rise to Address Output High Z for Flow-through Mode	1.00	7.20[34]	1.00	9.00[34]	1.00	11.00[34]	ns

Table 16.SDR Mode with Pipeline Mode, DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[33]

Parameter	Description	–200[27] Min.	–200[27] Max.	–167[27] Min.	–167[27] Max.	–133 Min.	–133 Max.	Unit
f_{MAX} (PIPELINED)	Maximum Operating Frequency for Pipelined Mode	100	250	100	200	100	167	MHz

Table 16.SDR Mode with Pipeline Mode, DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[33] (continued)

Parameter	Description		–200[27]		–167[27]		–133		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC} (PIPELINED)	C Clock Cycle Time for Pipelined Mode		4.00[34]	10.00	5.00[34]	10.00	6.00[34]	10.00	ns
t_{CKD}	C Clock Duty Time		45	55	45	55	45	55	%
t_{SD}	Data Input Set-up Time to C Rise	HSTL 1.8V LVCMOS	1.20[32,34]		1.50[32,34]		1.70[32,34]		ns
		2.5V LVCMOS 3.3V LVTTL	1.45[32,34]		1.75[32,34]		1.95[32,34]		ns
t_{HD}	Data Input Hold Time after C Rise		0.50		0.50		0.50		ns
t_{SAC}	Address & Control Input Set-up Time to C Rise	HSTL 1.8V LVCMOS	1.20[32,34]		1.50[32,34]		1.70[32,34]		ns
		2.5V LVCMOS 3.3V LVTTL	1.45[32,34]		1.75[32,34]		1.95[32,34]		ns
t_{HAC}	Address & Control Input Hold Time after C Rise		0.50		0.50		0.60		ns
t_{OE}	Output Enable to Data Valid			3.40[32,34]		4.40[32,34]		5.00[32,34]	ns
t_{OLZ}[31]	$\overline{\text{OE}}$ to Low Z		1.00		1.00		1.00		ns
t_{OHZ}[31]	$\overline{\text{OE}}$ to High Z		1.00	3.40[32,34]	1.00	4.40[32,34]	1.00	5.00[32,34]	ns
t_{CD2}[35]	C Rise to DQ Valid for Pipelined Mode (LowSPD = 1)			2.64[32,34]		3.30[32,34]		4.00[32,34]	ns
t_{CA2}	C Rise to Address Readback Valid for Pipelined Mode			4.00[34]		5.00[34]		6.00[34]	ns
t_{DC}[35]	DQ Output Hold after C Rise		1.00		1.00		1.00		ns
t_{CCQ}[35]	C Rise to CQ Rise		1.00	2.64[34]	1.00	3.30[34]	1.00	4.00[34]	ns
t_{CQHQV}[35]	Echo Clock (CQ) High to Output Valid	HSTL 1.8V LVCMOS		0.60[32]		0.70[32]		0.80[32]	ns
		2.5V LVCMOS 3.3V LVTTL		0.70[32]		0.80[32]		0.90[32]	ns
t_{CQHQX}[35]	Echo Clock (CQ) High to Output Hold	HSTL 1.8V LVCMOS	–0.60		–0.70		–0.80		ns
		2.5V LVCMOS 3.3V LVTTL	–0.75		–0.85		–0.95		ns
t_{CKHZ2}[31,35]	C Rise to DQ Output High Z in Pipelined Mode		1.00	2.64 [32, 34]	1.00	3.30[32,34]	1.00	4.00[32,34]	ns
t_{CKLZ2}[31,35]	C Rise to DQ Output Low Z in Pipelined Mode		1.00		1.00		1.00		ns
t_{AC}	Address Output Hold after C Rise		1.00		1.00		1.00		ns
t_{CKHZA2}[31]	C Rise to Address Output High Z for Pipelined Mode		1.00	4.00[34]	1.00	5.00[34]	1.00	6.00[34]	ns
t_{CKLZA}[31]	C Rise to Address Output Low Z		1.00		1.00		1.00		ns
t_{SCINT}	C Rise to $\overline{\text{CNTINT}}$ Low		1.00	2.64[34]	1.00	3.30[34]	1.00	4.00[34]	ns
t_{RCINT}	C Rise to $\overline{\text{CNTINT}}$ High		1.00	2.64[34]	1.00	3.30[34]	1.00	4.00[34]	ns
t_{SINT}	C Rise to $\overline{\text{INT}}$ Low		0.50	6.00[34]	0.50	7.00[34]	0.50	8.00[34]	ns
t_{RINT}	C Rise to $\overline{\text{INT}}$ High		0.50	6.00[34]	0.50	7.00[34]	0.50	8.00[34]	ns
t_{BSY}	C Rise to $\overline{\text{BUSY}}$ Valid		1.00	2.64[34]	1.00	3.30[34]	1.00	4.00[34]	ns
t_{JIT}	Clock Input Cycle to Cycle Jitter			+/- 200		+/- 200		+/- 200	ps

Table 17.SDR Mode with Pipeline Mode, DLL Disabled ($\overline{\text{LOWSPD}}$-LOW)[33]

Parameter	Description		All Speed Bins		Unit
			Min.	Max.	
f_{MAX} (PIPELINED)	Maximum Operating Frequency for Pipelined Mode			100	MHz
t_{CYC} (PIPELINED)	C Clock Cycle Time for Pipelined Mode		10.00[34]		ns
t_{CKD}	C Clock Duty Time		45	55	%
t_{SD}	Data Input Set-up Time to C Rise	HSTL 1.8V LVCMOS	1.80[32,34]		ns
		2.5V LVCMOS 3.3V LVTTL	2.05[32,34]		ns
t_{HD}	Data Input Hold Time after C Rise		0.50		ns
t_{SAC}	Address & Control Input Set-up Time to C Rise	HSTL 1.8V LVCMOS	1.80[32,34]		ns
		2.5V LVCMOS 3.3V LVTTL	2.05[32,34]		ns
t_{HAC}	Address & Control Input Hold Time after C Rise		0.70		ns
t_{OE}	Output Enable to Data Valid			5.50[32,34]	ns
t_{OLZ}[31]	$\overline{\text{OE}}$ to Low Z		1.00		ns
t_{OHZ}[31]	$\overline{\text{OE}}$ to High Z		1.00	5.50[32,34]	ns
t_{CD2}[35]	C Rise to DQ Valid for Pipelined Mode ($\overline{\text{LowSPD}}$ = 0)			6.00[32,34]	ns
t_{CA2}	C Rise to Address Readback Valid for Pipelined Mode			7.50[34]	ns
t_{DC}[35]	DQ Output Hold after C Rise		1.00		ns
t_{CCQ}[35]	C Rise to CQ Rise		1.00	6.00[34]	ns
t_{CQHQV}[35]	Echo Clock (CQ) High to Output Valid	HSTL 1.8V LVCMOS		0.90[32]	ns
		2.5V LVCMOS 3.3V LVTTL		1.00[32]	ns
t_{CQHQX}[35]	Echo Clock (CQ) High to Output Hold	HSTL 1.8V LVCMOS	–0.90		ns
		2.5V LVCMOS 3.3V LVTTL	–1.05		ns
t_{CKHZ2}[31,35]	C Rise to DQ Output High Z in Pipelined Mode		1.00	6.00[32,34]	ns
t_{CKLZ2}[31,35]	C Rise to DQ Output Low Z in Pipelined Mode		1.00		ns
t_{AC}	Address Output Hold after C Rise		1.00		ns
t_{CKHZA2}[31]	C Rise to Address Output High Z for Pipelined Mode		1.00	7.50[34]	ns
t_{CKLZA}[31]	C Rise to Address Output Low Z		1.00		ns
t_{SCINT}	C Rise to $\overline{\text{CNTINT}}$ Low		1.00	4.50[34]	ns
t_{RCINT}	C Rise to $\overline{\text{CNTINT}}$ High		1.00	4.50[34]	ns
t_{SINT}	C Rise to $\overline{\text{INT}}$ Low		0.50	8.50[34]	ns
t_{RINT}	C Rise to $\overline{\text{INT}}$ High		0.50	8.50[34]	ns
t_{BSY}	C Rise to $\overline{\text{BUSY}}$ Valid		1.00	4.50[34]	ns

Table 18.Master Reset Timing

Parameter	Description	–200[27]		–167[27]		–133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PUP}	Power-up Time	1		1		1		ms
t_{RS}	Master Reset Pulse Width	5		5		5		cycles

Table 18.Master Reset Timing

Parameter	Description	–200[27]		–167[27]		–133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSR}	Master Reset Recovery Time	5		5		5		cycles
t_{RSF}	Master Reset to Outputs Inactive/Hi-Z		12		15		18	ns
t_{RDY}[37]	Master Reset Release to Port Ready		1024		1024		1024	cycles
t_{CORDY}[38]	C Rise to Port Ready		8[34]		9.5[34]		11[34]	ns

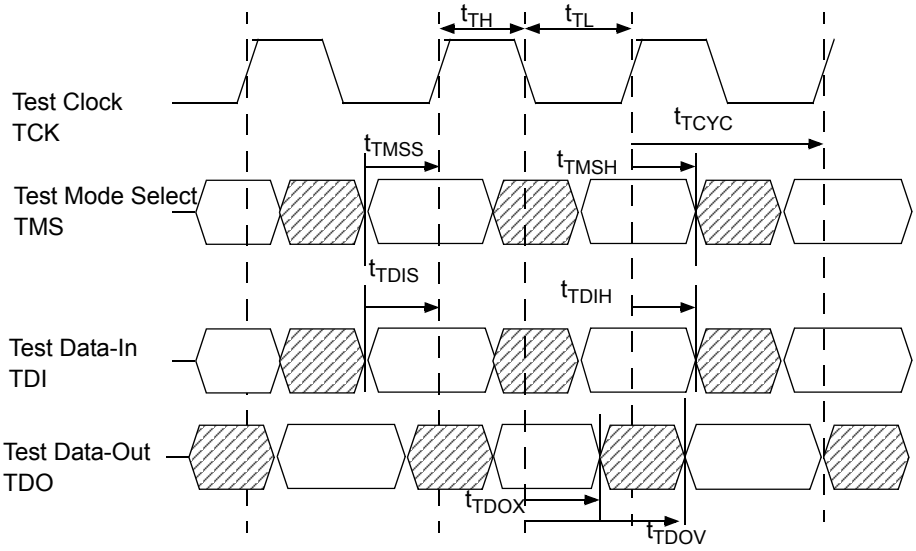
Table 19.JTAG Timing

Parameter	Description	–200[27]		–167[27]		–133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{JTAG}	JTAG TAP Controller Frequency		20		20		20	MHz
t_{TCYC}	TCK Cycle Time	50		50		50		ns
t_{TH}	TCK High Time	20		20		20		ns
t_{TL}	TCK Low Time	20		20		20		ns
t_{TMSS}	TMS Set-up to TCK Rise	10		10		10		ns
t_{TMSH}	TMS Hold to TCK Rise	10		10		10		ns
t_{TDIS}	TDI Set-up to TCK Rise	10		10		10		ns
t_{TDIH}	TDI Hold to TCK Rise	10		10		10		ns
t_{TDOV}	TCK Low to TDO Valid		10		10		10	ns
t_{TDOX}	TCK Low to TDO Invalid	0		0		0		ns
t_{JXZ}	TCK Low to TDO hi-Z		15		15		15	ns
t_{JZX}	TCK Low to TDO Active		15		15		15	ns

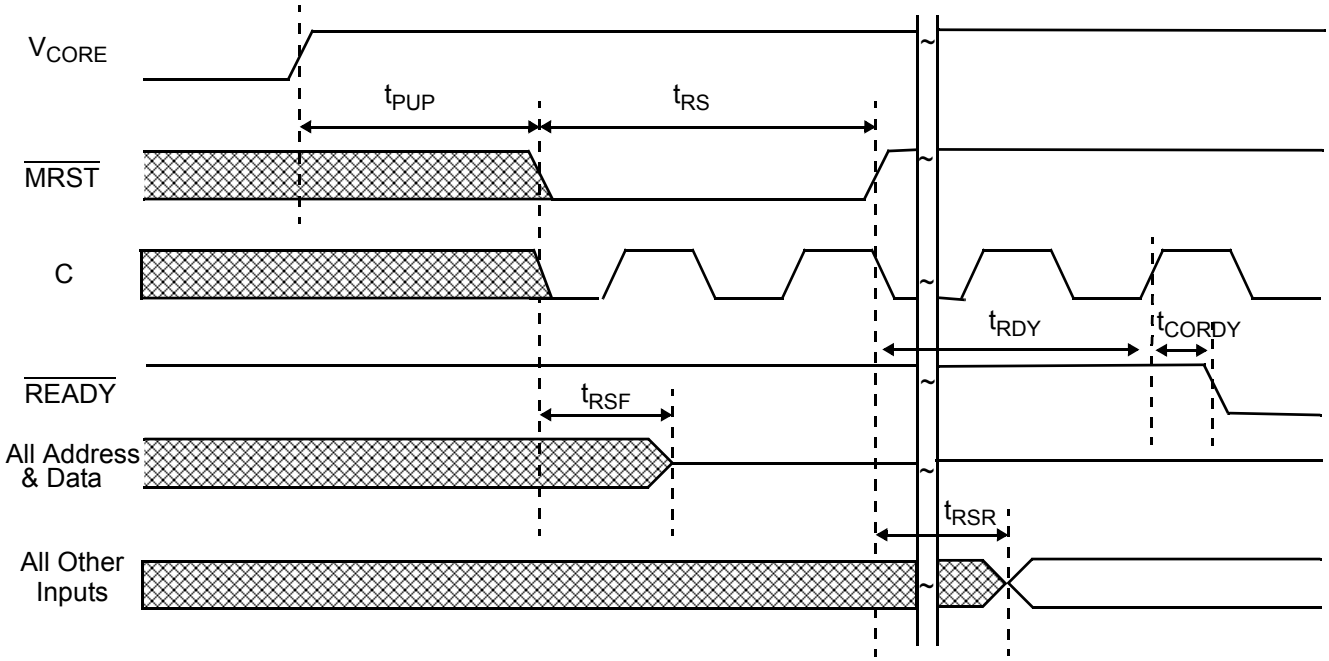
Notes:
37. $\overline{\text{READY}}$ is a wired OR capable output with a weak pull-down. For a decreased falling delay, connect a 250 Ω resistor to VSS.
38. Add this propagation delay after t_{RDY} for all Master Reset Operations

Switching Waveforms

JTAG Timing

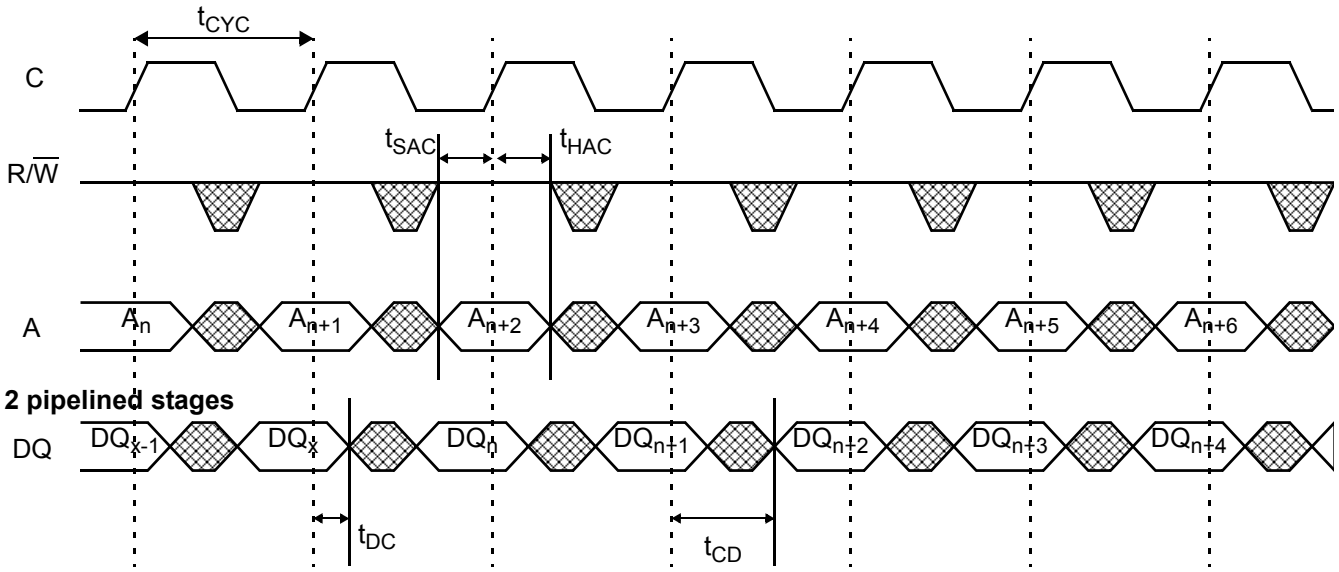


Master Reset[37]

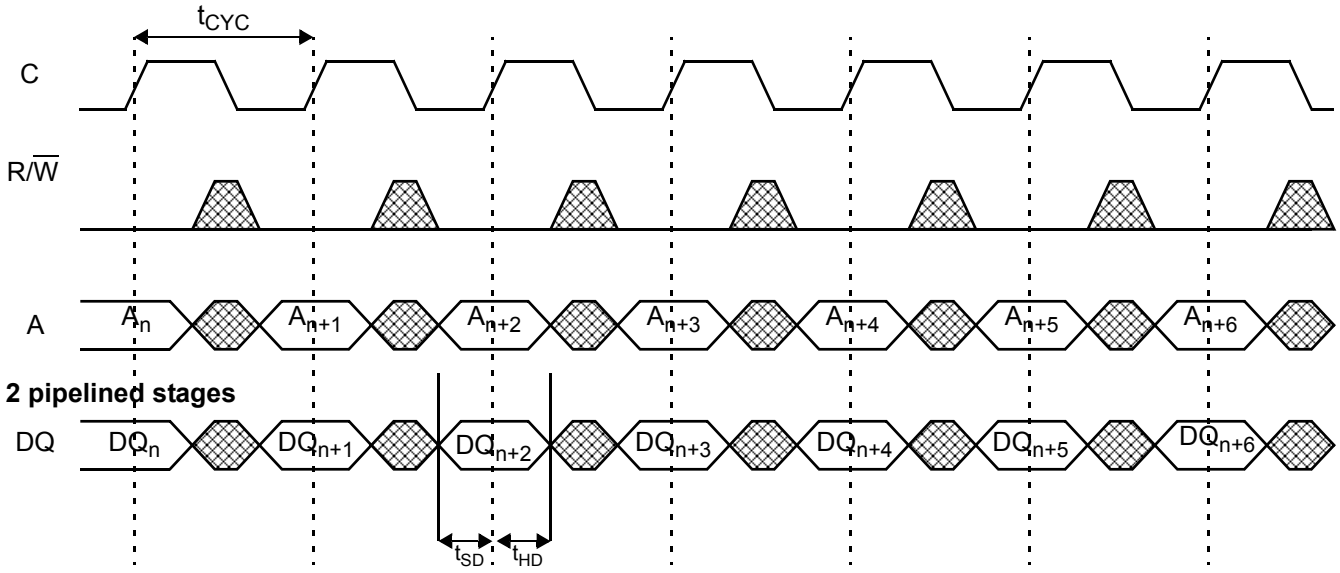


Switching Waveforms (continued)

READ Cycle for Pipelined Mode, DDRON = LOW

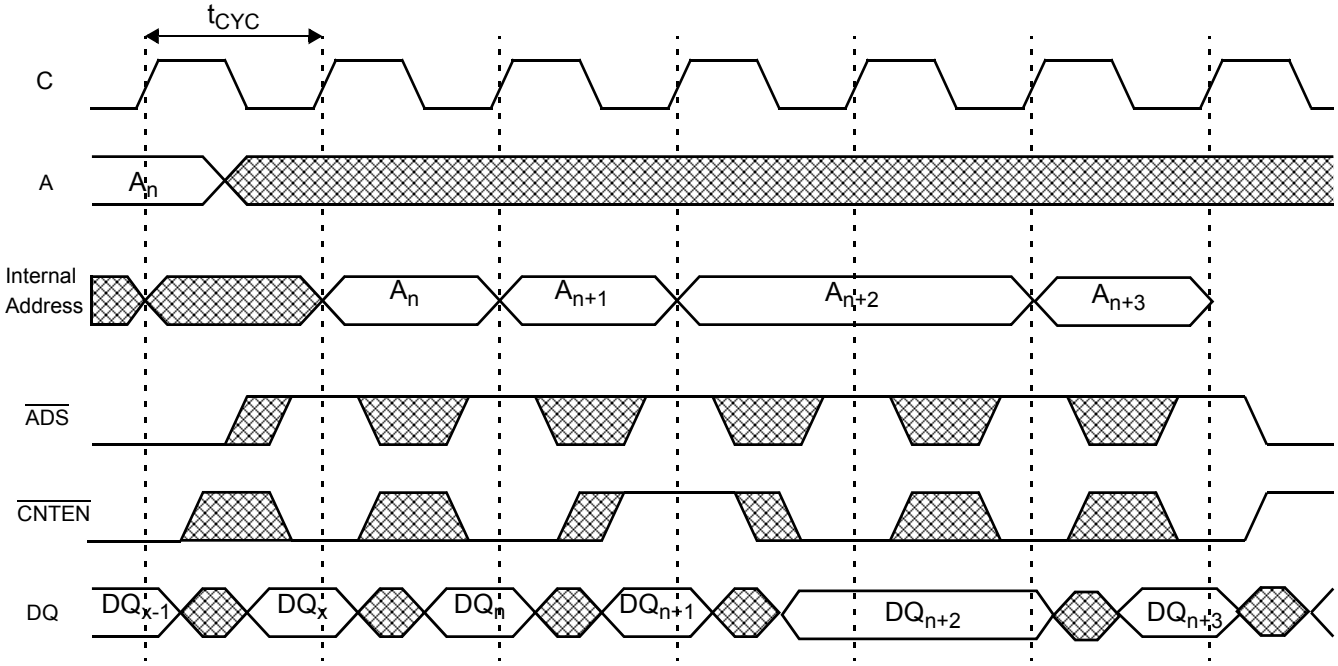


WRITE Cycle for Pipelined and Flow-through Modes, DDRON = LOW

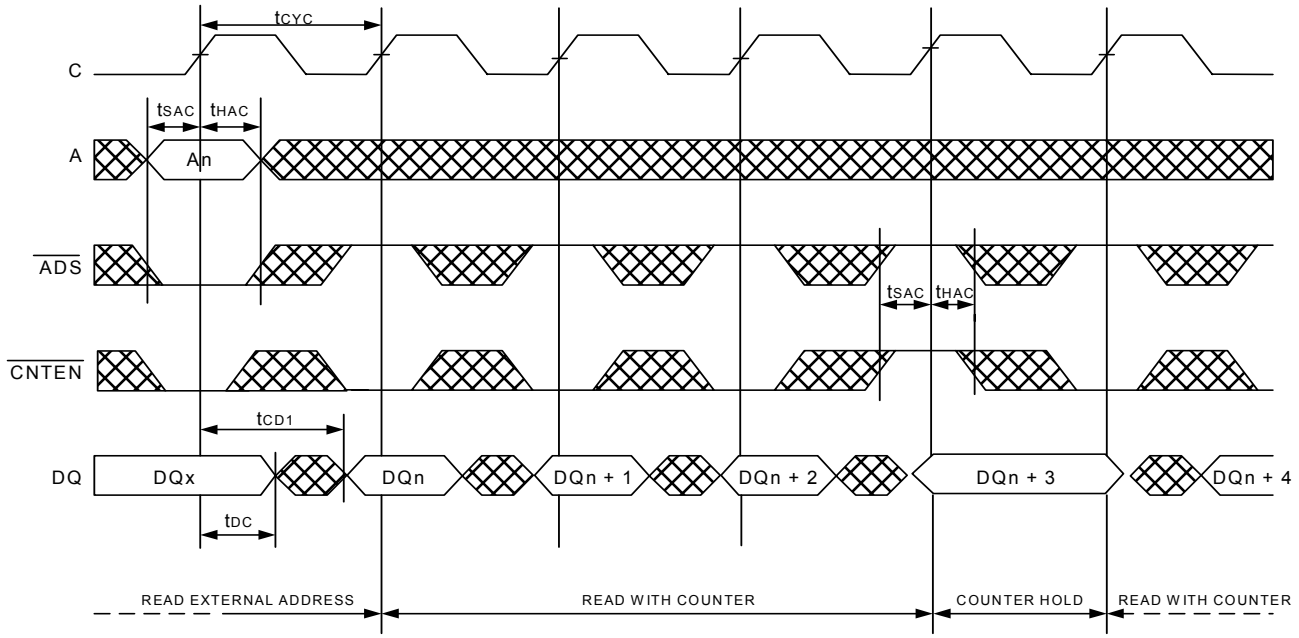


Switching Waveforms (continued)

READ with Address Counter Advance for Pipelined Mode, DDRON = LOW

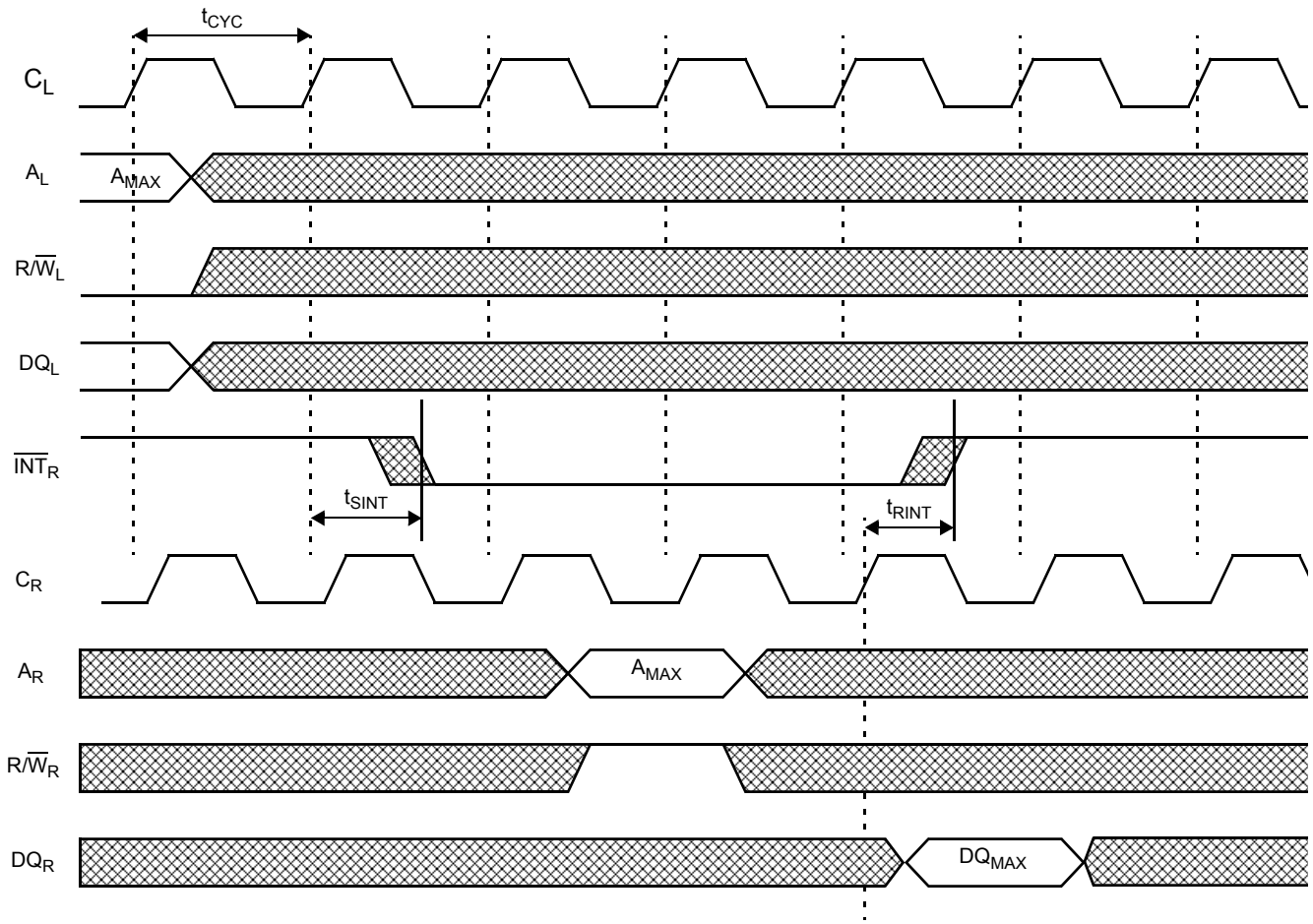


READ with Address Counter Advance for Flow-through Mode, DDRON = LOW



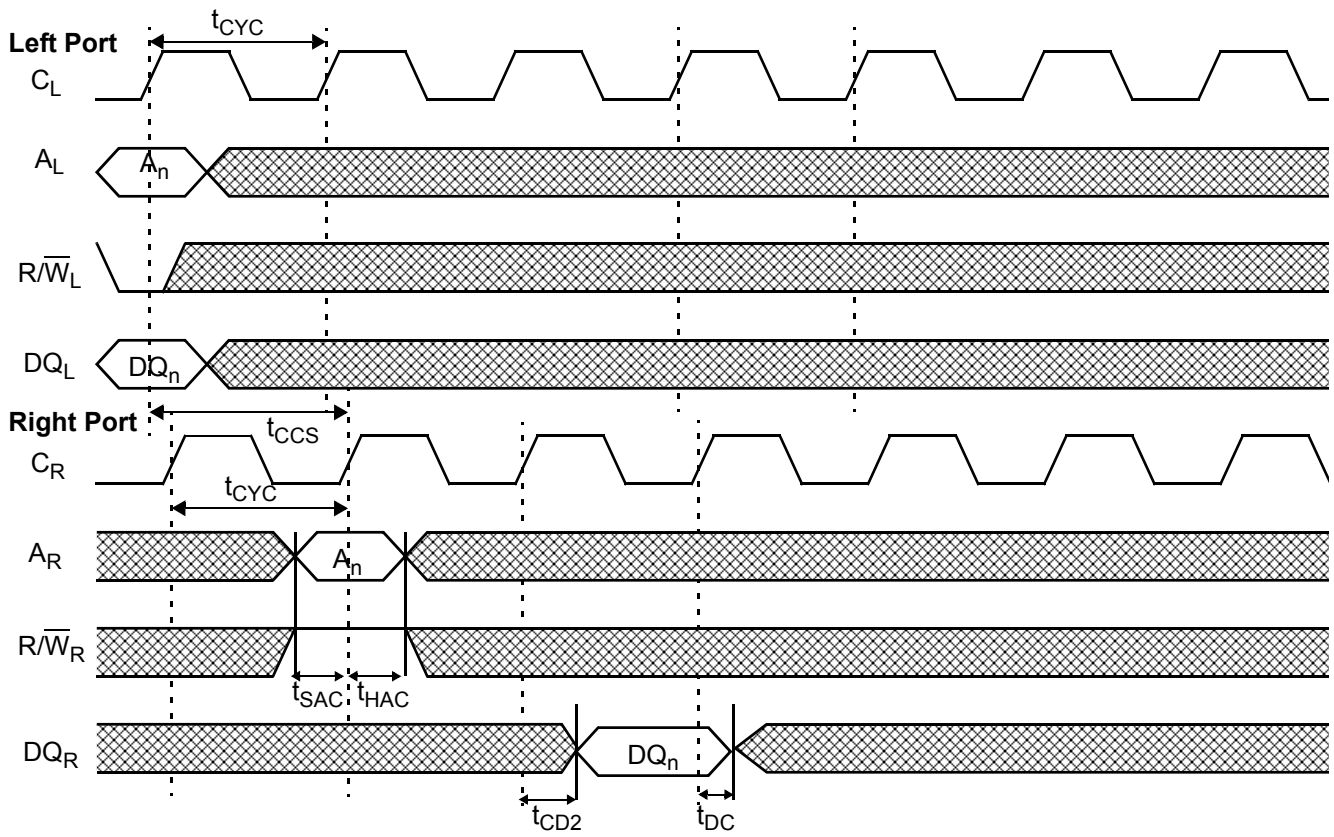
Switching Waveforms (continued)

Mailbox Interrupt Output, DDRON = LOW

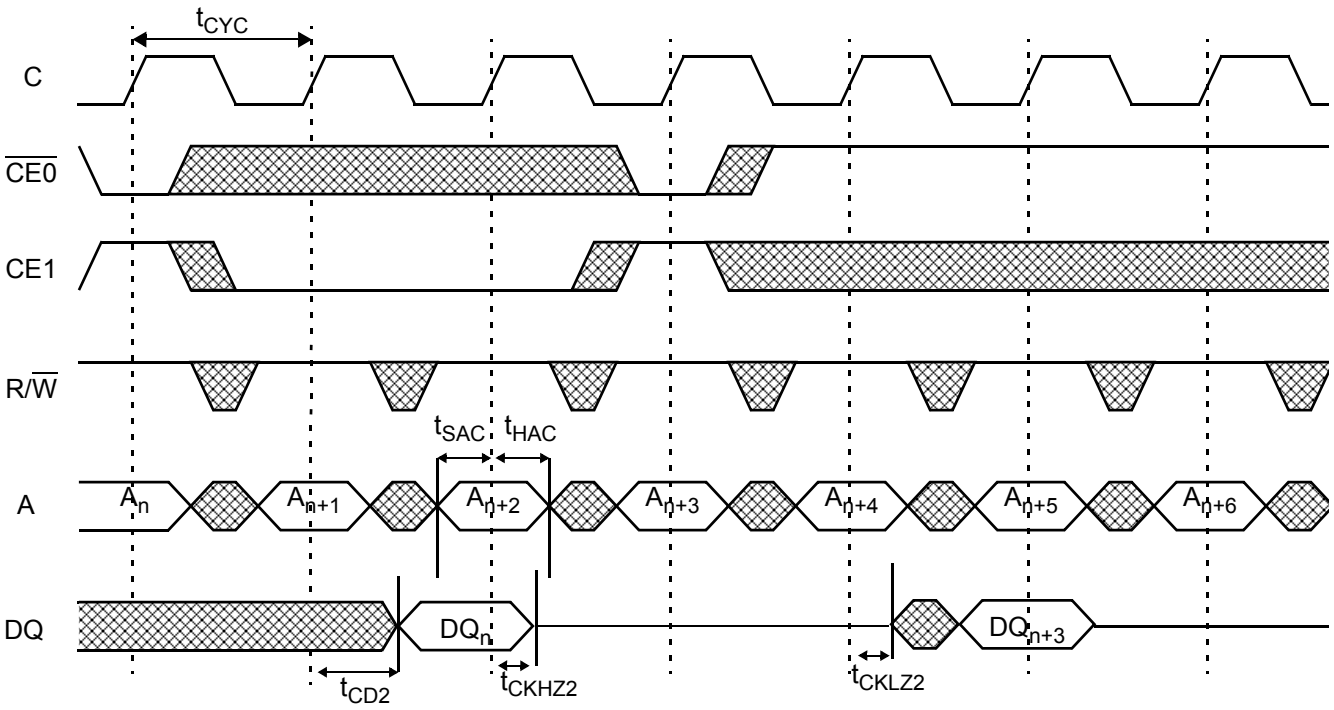


Switching Waveforms (continued)

Port-to-Port WRITE–READ for Pipelined Mode, DDRON = LOW

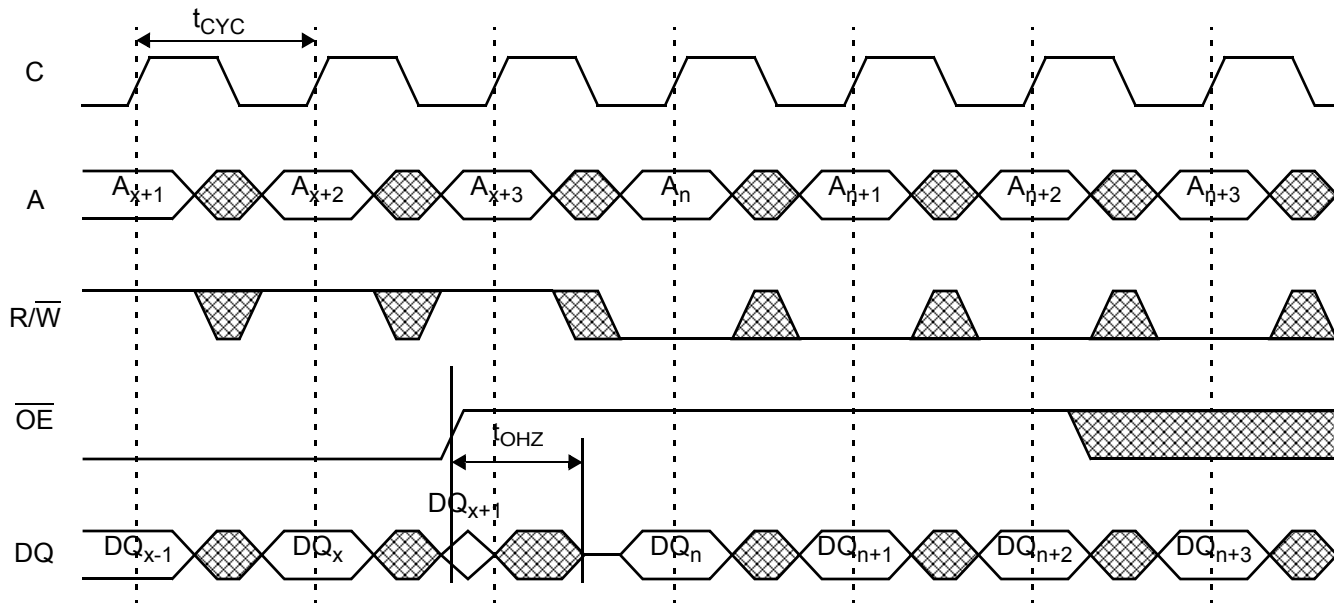


Chip Enable READ for Pipelined Mode, DDRON = LOW

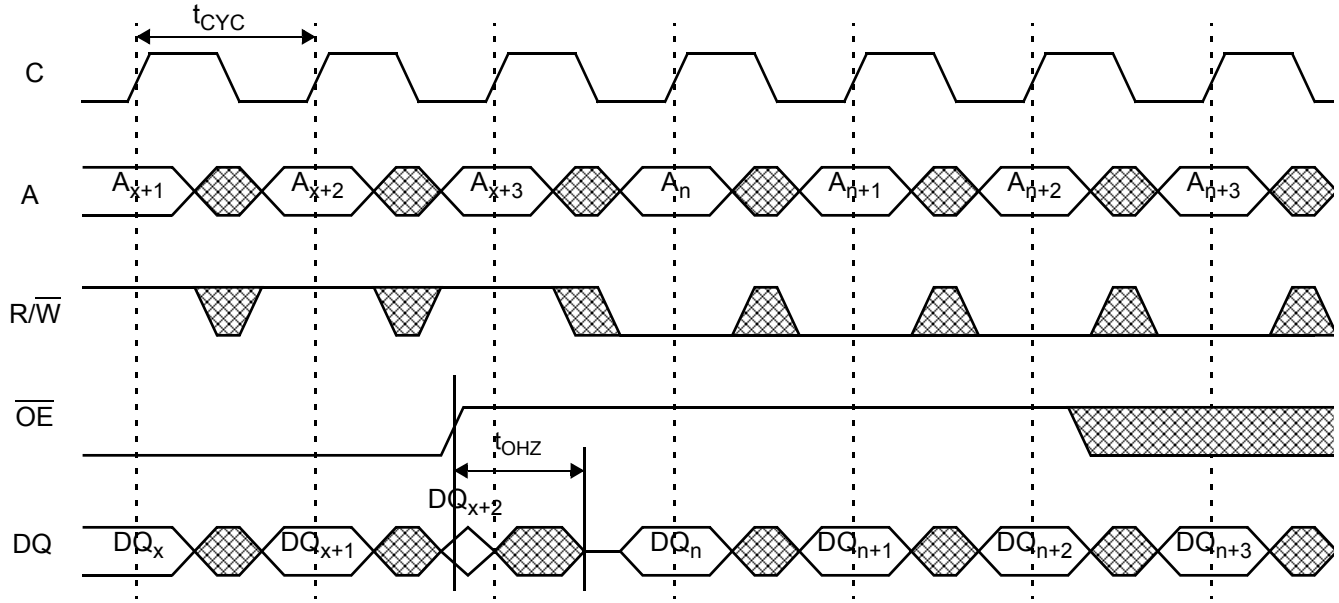


Switching Waveforms (continued)

OE Controlled WRITE for Pipelined Mode, DDRON = LOW

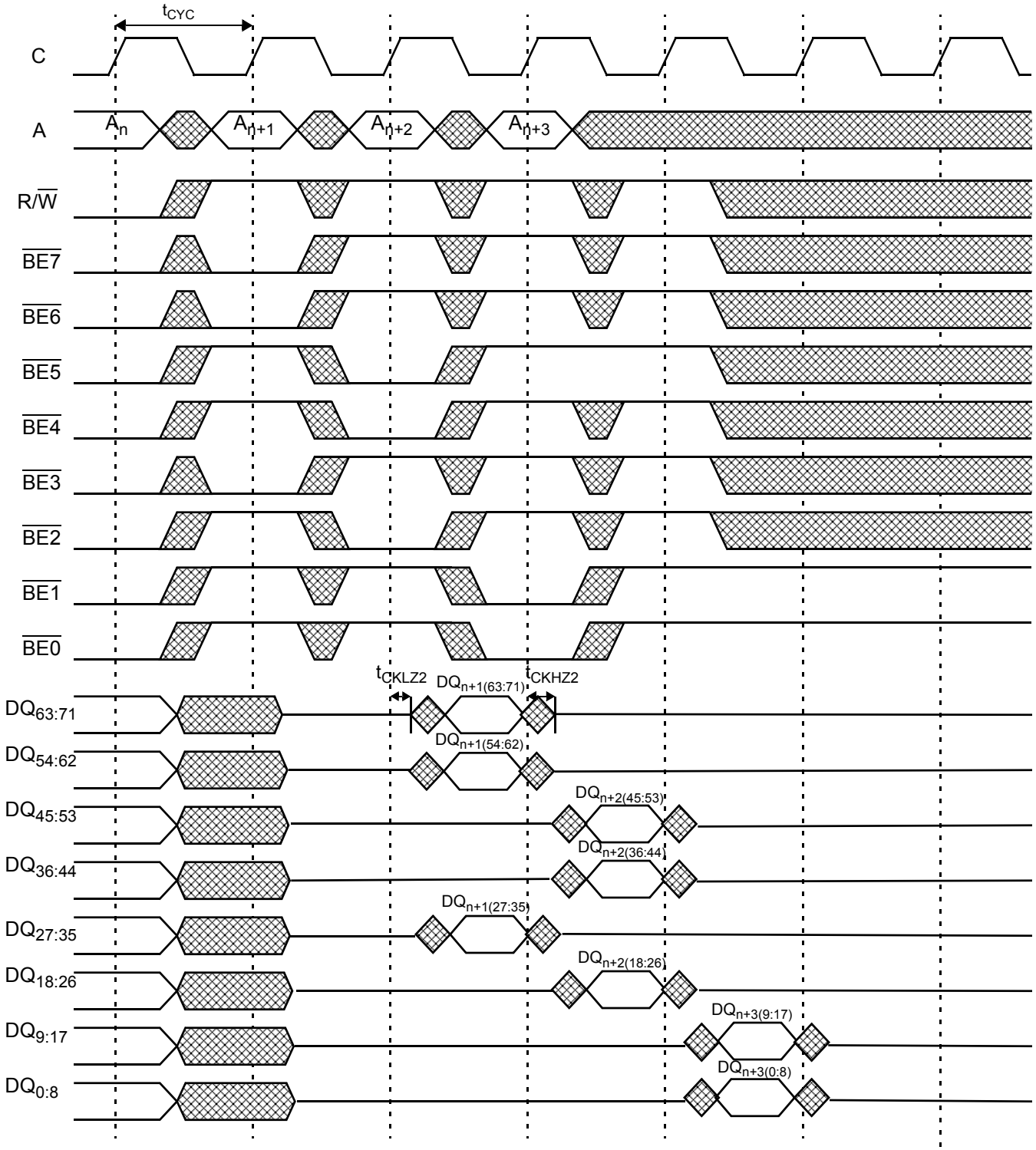


OE Controlled WRITE for Flow-through Mode, DDRON = LOW



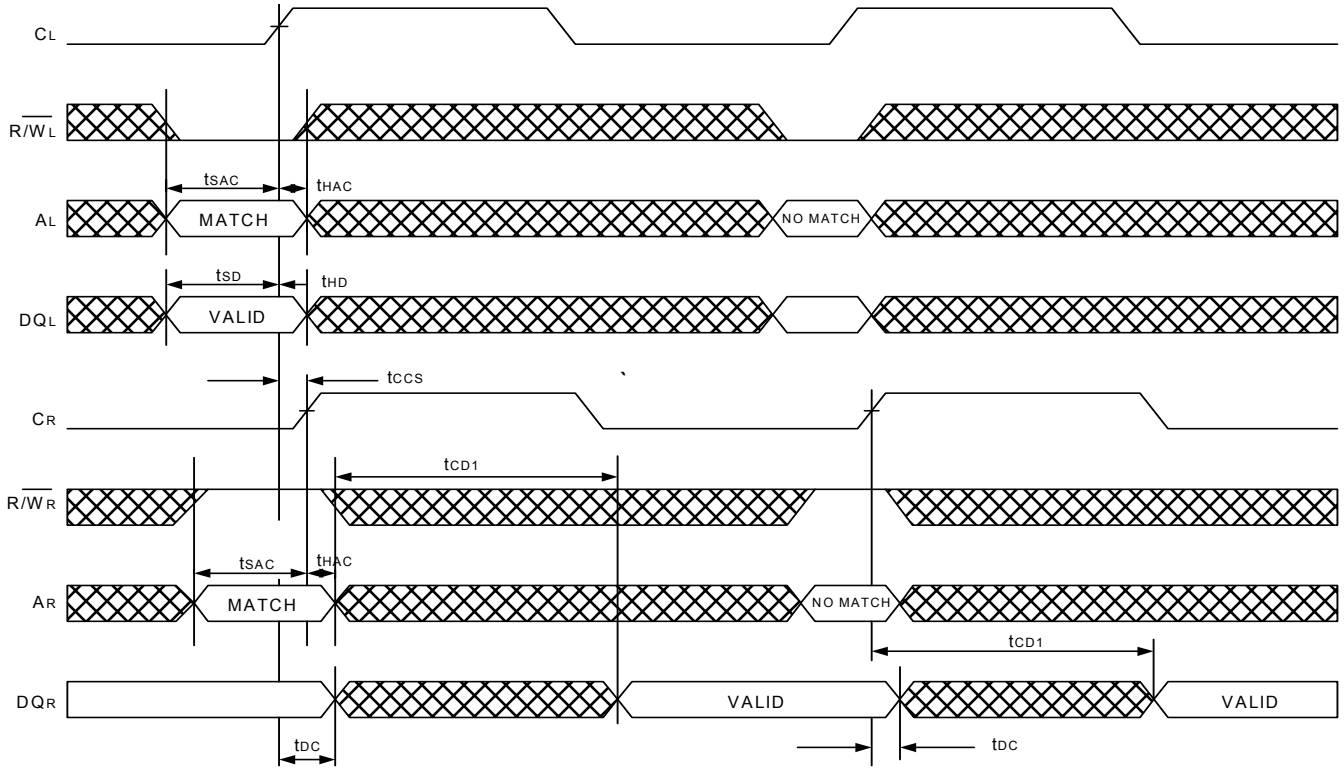
Switching Waveforms (continued)

Byte-Enable READ for Pipelined Mode, DDRON = LOW

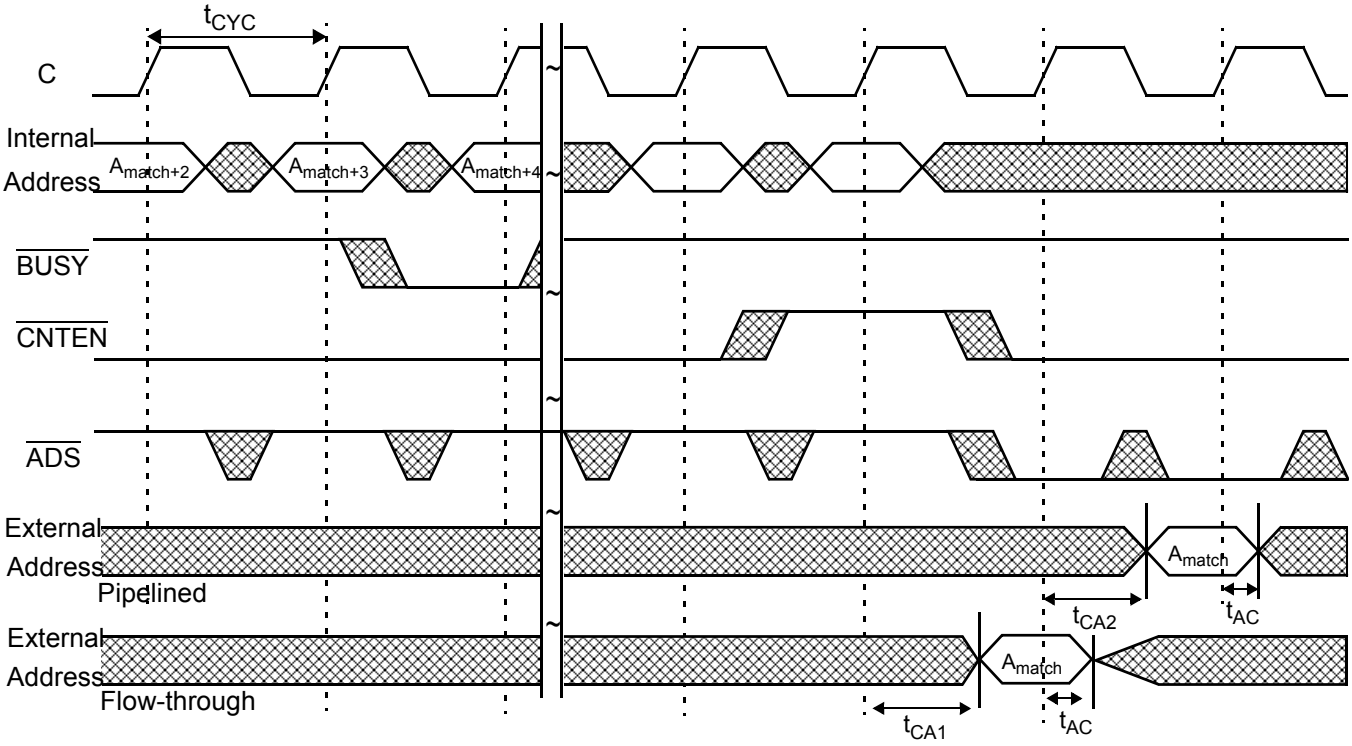


Switching Waveforms (continued)

Port-to-Port WRITE-to-READ for Flow-through Mode, DDRON = LOW



BUSY Address Readback for Pipelined and Flow-through Modes, DDRON = CNT/MSK = RET = LOW[39]

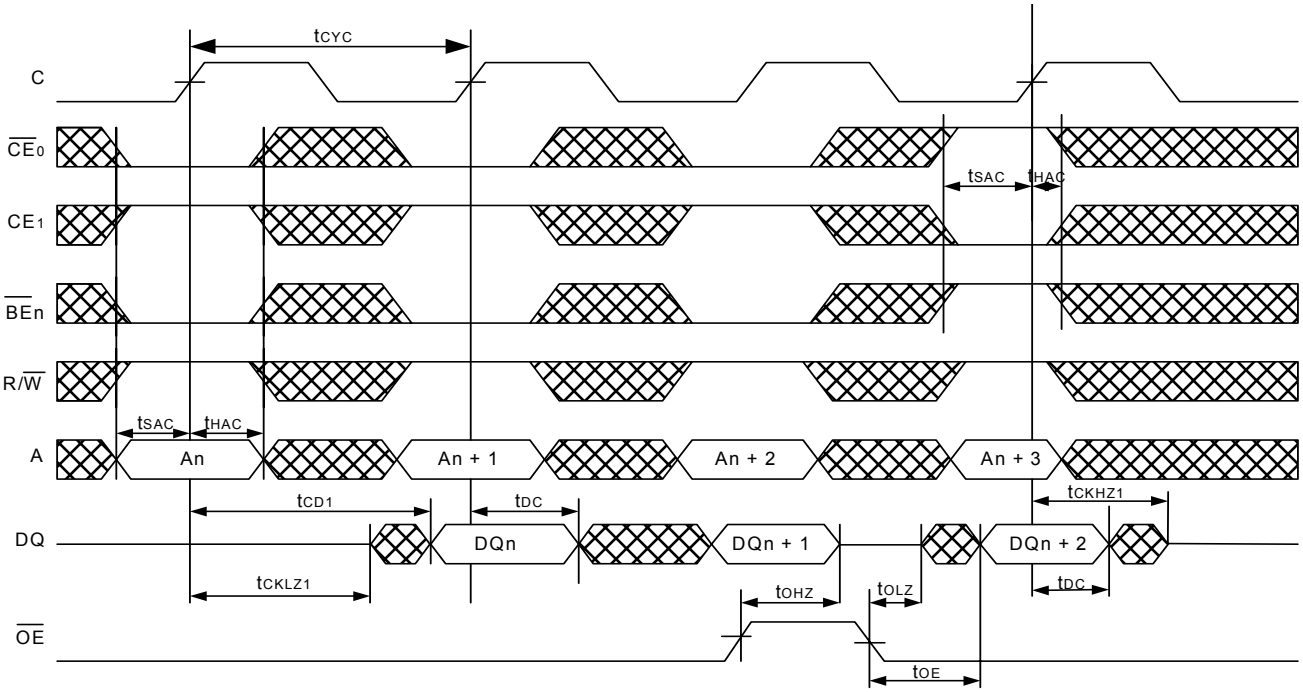


Note:

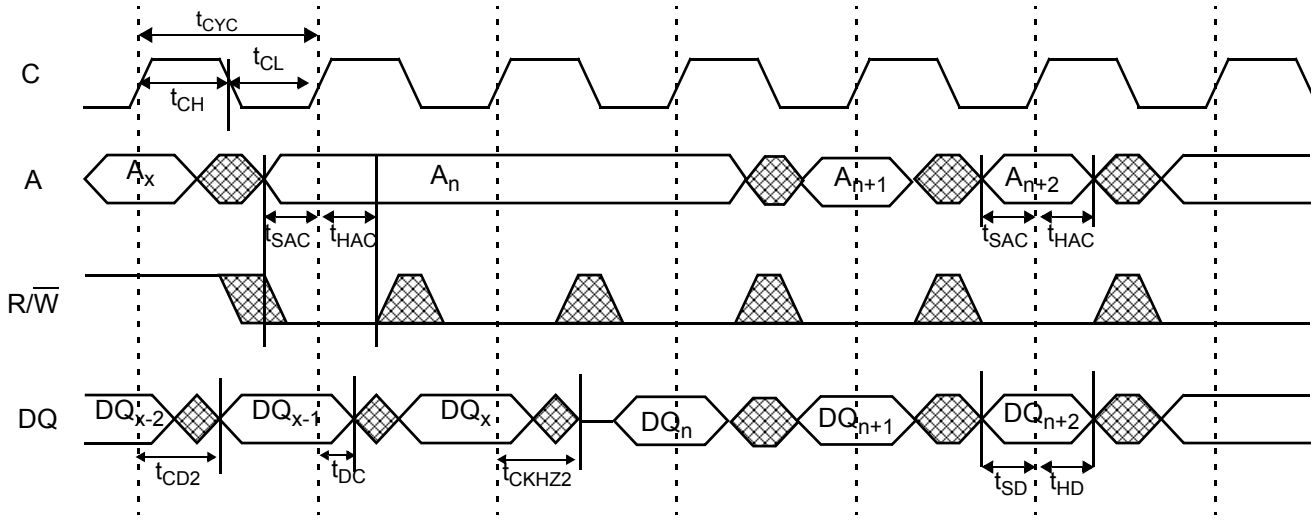
39. A_{match} is the matching address which will be reported on the address bus of the losing port. The counter operation selected for reporting the address is "Busy Address Readback."

Switching Waveforms (continued)

Read Cycle for Flow-through Mode, DDRON = LOW



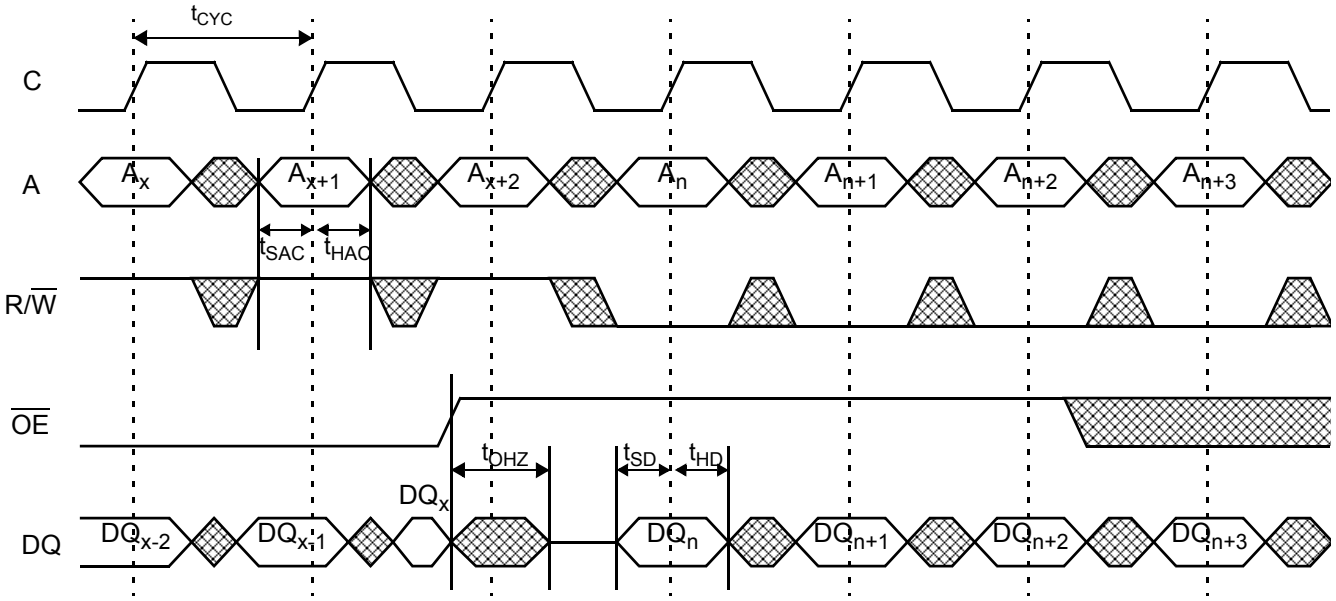
READ-to-WRITE for Pipelined Mode, DDRON = LOW (OE = V_{IL})[40, 41, 42]



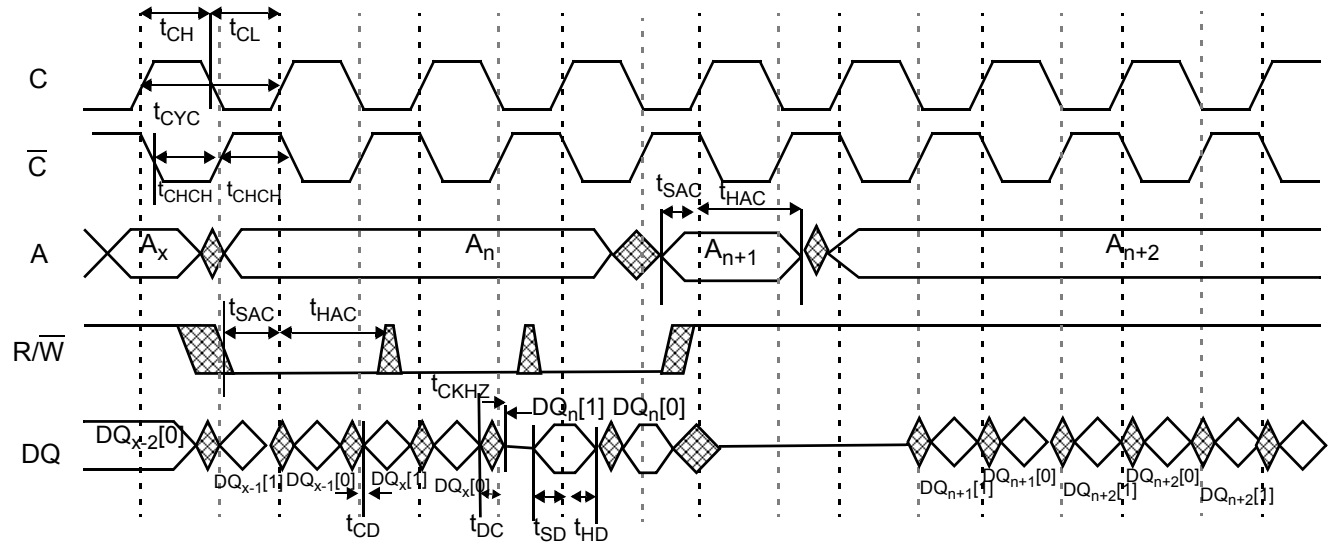
Notes:
40. When $\overline{OE}$ = V_{IL}, the last read operation is allowed to complete before the DQ bus is tri-stated and the user is allowed to drive write data.
41. Two dummy writes should be issued to accomplish bus turnaround. The third instruction is the first valid write.
42. Chip enable or all byte enables should be held inactive during the two dummy writes to avoid data corruption.

Switching Waveforms (continued)

READ-to-WRITE for Pipelined Mode, DDRON = LOW ($\overline{OE}$ Controlled)[43, 44]



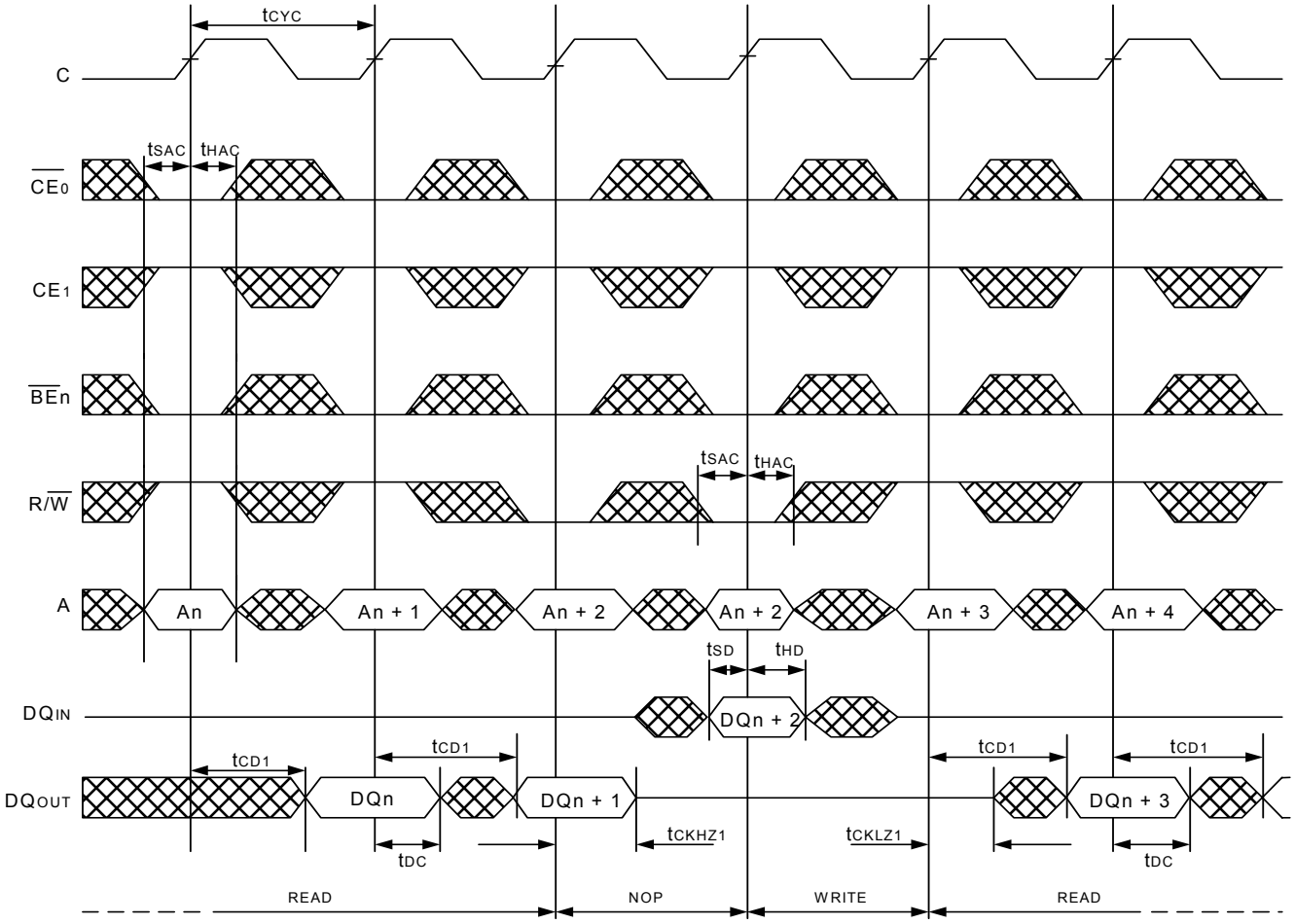
READ-to-WRITE-to-READ for DDR, DDRON = HIGH[40,41,45,46]



Notes:
43. $\overline{OE}$ should be deasserted and t_{OHZ} allowed to elapse before the first write operation is issued.
44. Any write scheduled to complete after $\overline{OE}$ is deasserted will be preempted.
45. The address should be held constant during the two dummy writes and first valid write to avoid data corruption.
46. D[1]/Q [1] contains data [71:36]; D[0]/Q[0] contains data [35:0].

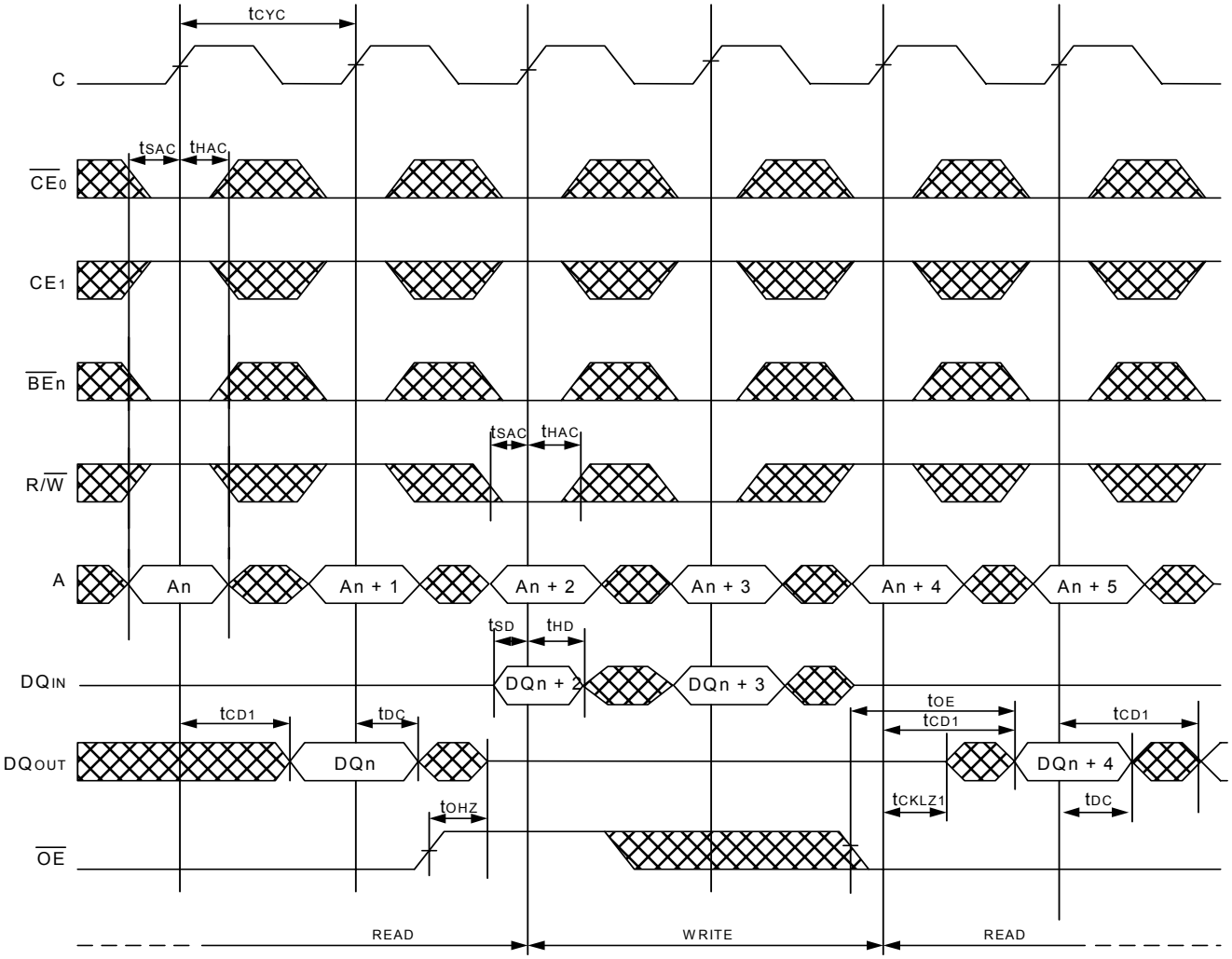
Switching Waveforms (continued)

Read-to-Write-to-Read for Flow-through Mode, DDRON = LOW ($\overline{OE}$ = LOW)



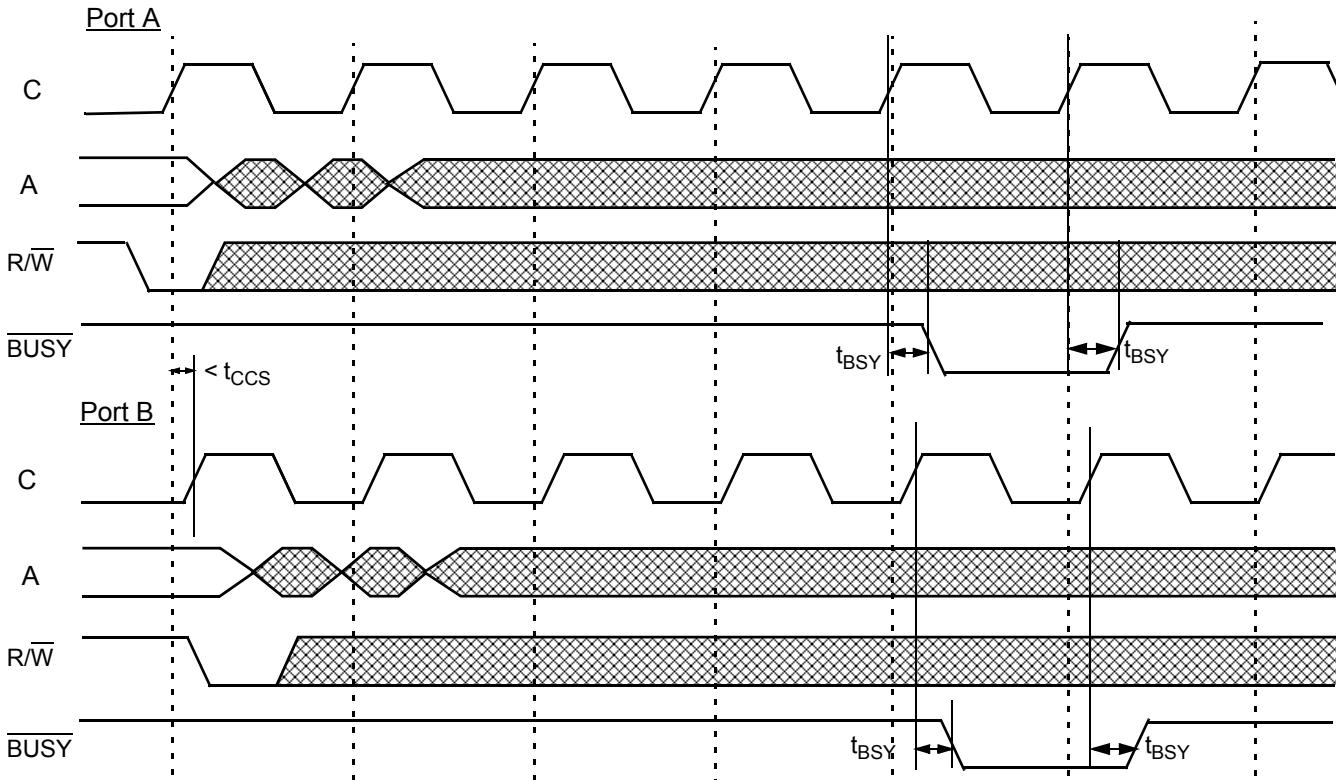
Switching Waveforms (continued)

Read-to-Write-to-Read for Flow-through Mode, DDRON = LOW ($\overline{OE}$ Controlled)

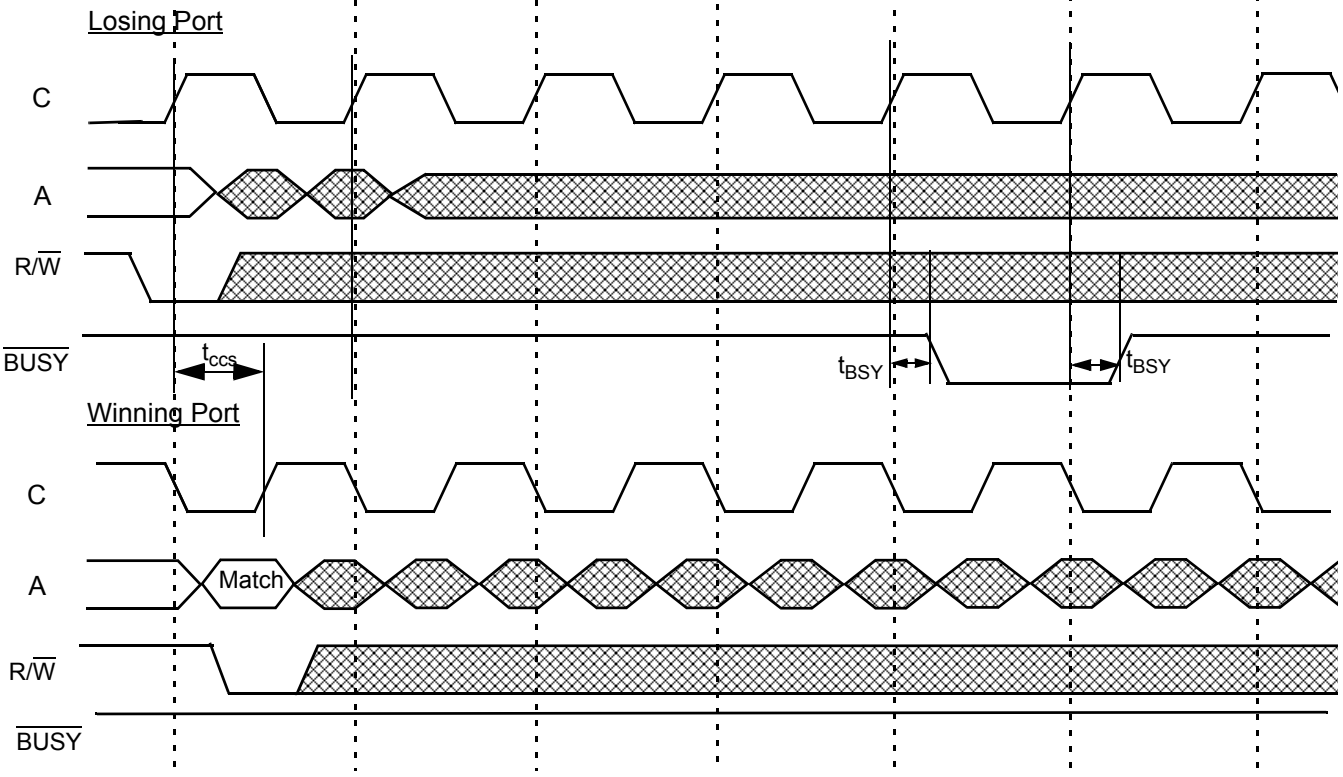


Switching Waveforms (continued)

$\overline{BUSY}$ Timing, WRITE-WRITE Collision for Pipelined and Flow-through Modes, Clock Timing Violates t_{CCS}. (Flag Both Ports)

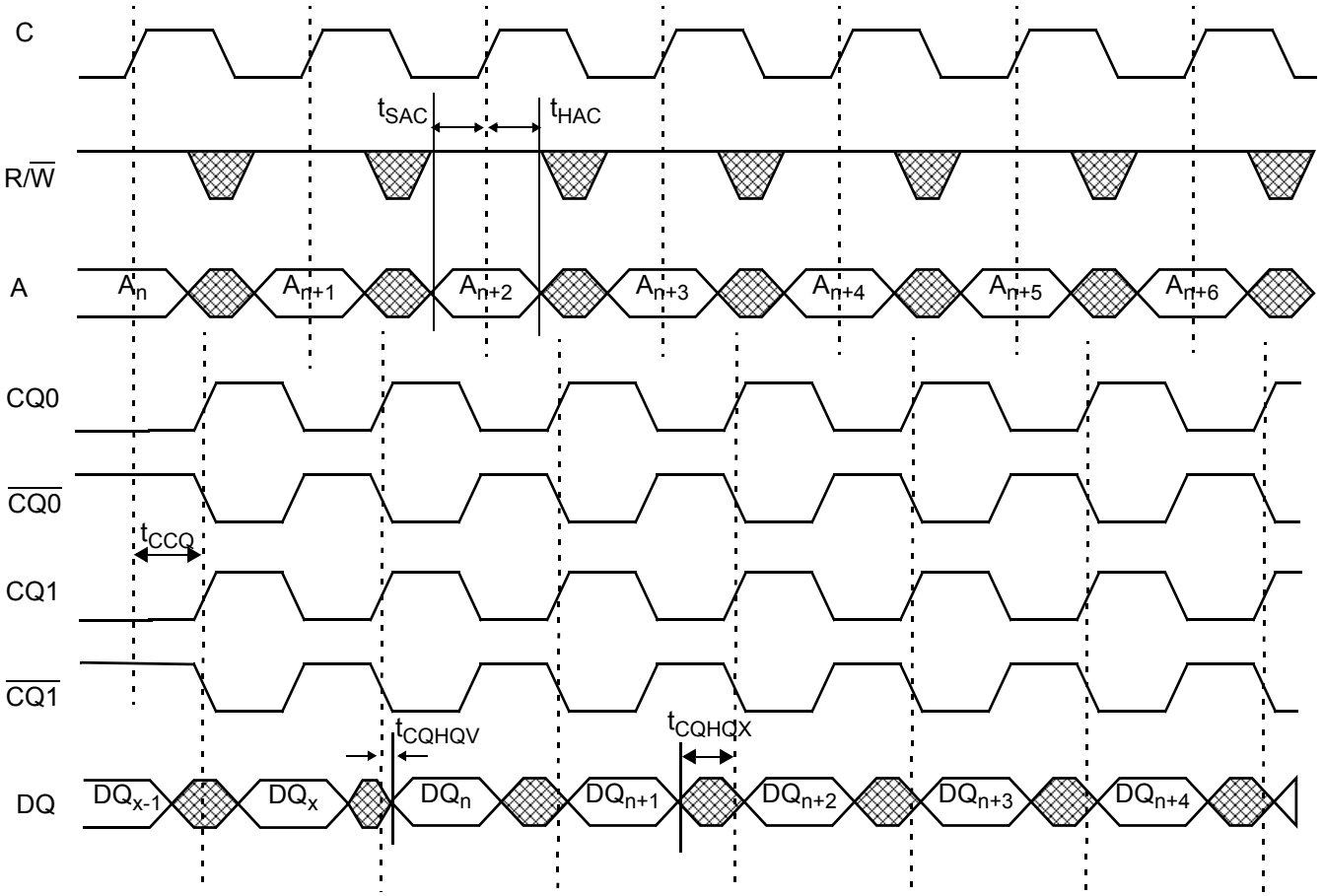


$\overline{BUSY}$ Timing, WRITE-WRITE Collision for Pipelined and Flow-through Modes, Clock Timing Meets t_{CCS}. (Flag Losing Port)



Switching Waveforms (continued)

Read with Echo Clock for Pipelined Mode (CQEN = HIGH)



Ordering Information

256K × 72/256K × 36 × 2 (18 Mbit) 1.8V/1.5V Synchronous CYDD18S72V18 Dual-Port SRAM (SDR and DDR I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD18S72V18-200BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S72V18-200BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD18S72V18-167BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S72V18-167BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD18S72V18-167BGXI	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD18S72V18-167BGI	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Industrial

128K × 72/128K × 36 × 2 (9 Mbit) 1.8V/1.5V Synchronous CYDD09S72V18 Dual-Port SRAM (SDR and DDR I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD09S72V18-200BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S72V18-200BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD09S72V18-167BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S72V18-167BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD09S72V18-167BGXI	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD09S72V18-167BGI	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Industrial

64K × 72/64K × 36 × 2 (4 Mbit) 1.8V/1.5V Synchronous CYDD04S72V18 Dual-Port SRAM (SDR and DDR I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD04S72V18-200BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S72V18-200BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD04S72V18-167BGXC	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S72V18-167BGC	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD04S72V18-167BGXI	BY484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD04S72V18-167BGI	BG484A	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Leaded)	Industrial

1024K × 36 × 2 (36 Mbit) 1.8V/1.5V Synchronous CYDD36S36V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYDD36S36V18-167BGXC	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD36S36V18-167BGC	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Commercial
133	CYDD36S36V18-133BGXC	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD36S36V18-133BGC	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD36S36V18-133BGXI	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD36S36V18-133BGI	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Industrial

Ordering Information (continued)

512K × 36 × 2 (18 Mbit) 1.8V/1.5V Synchronous CYDD18S36V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD18S36V18-200BBXC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S36V18-200BBC	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD18S36V18-167BBXC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S36V18-167BBC	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD18S36V18-167BBXI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD18S36V18-167BBI	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Industrial

256K × 36 × 2 (9 Mbit) 1.8V/1.5V Synchronous CYDD09S36V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD09S36V18-200BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S36V18-200BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD09S36V18-167BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S36V18-167BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD09S36V18-167BBXI	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD09S36V18-167BBI	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Industrial

128K × 36 × 2 **(4 Mbit) 1.8V/1.5V Synchronous CYDD04S36V18 Dual-Port SRAM (DDR only I/O)**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD04S36V18-200BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S36V18-200BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD04S36V18-167BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S36V18-167BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD04S36V18-167BBXI	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD04S36V18-167BBI	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Industrial

2048K × 18 × 2 (36 Mbit) 1.8V/1.5V Synchronous CYDD36S18V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYDD36S18V18-167BGXC	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD36S18V18-167BGC	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Commercial
133	CYDD36S18V18-133BGXC	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD36S18V18-133BGC	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD36S18V18-133BGXI	BY484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD36S18V18-133BGI	BG484S	484-ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Leaded)	Industrial

1024K × 18 × 2 (18 Mbit) 1.8V/1.5V Synchronous CYDD18S18V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD18S18V18-200BBXC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S18V18-200BBC	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD18S18V18-167BBXC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD18S18V18-167BBC	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD18S18V18-167BBXI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD18S18V18-167BBI	BB256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (Leaded)	Industrial

Ordering Information (continued)

512K × 18 × 2 (9 Mbit) 1.8V/1.5V Synchronous CYDD09S18V18 Dual-Port SRAM (DDR only I/O)

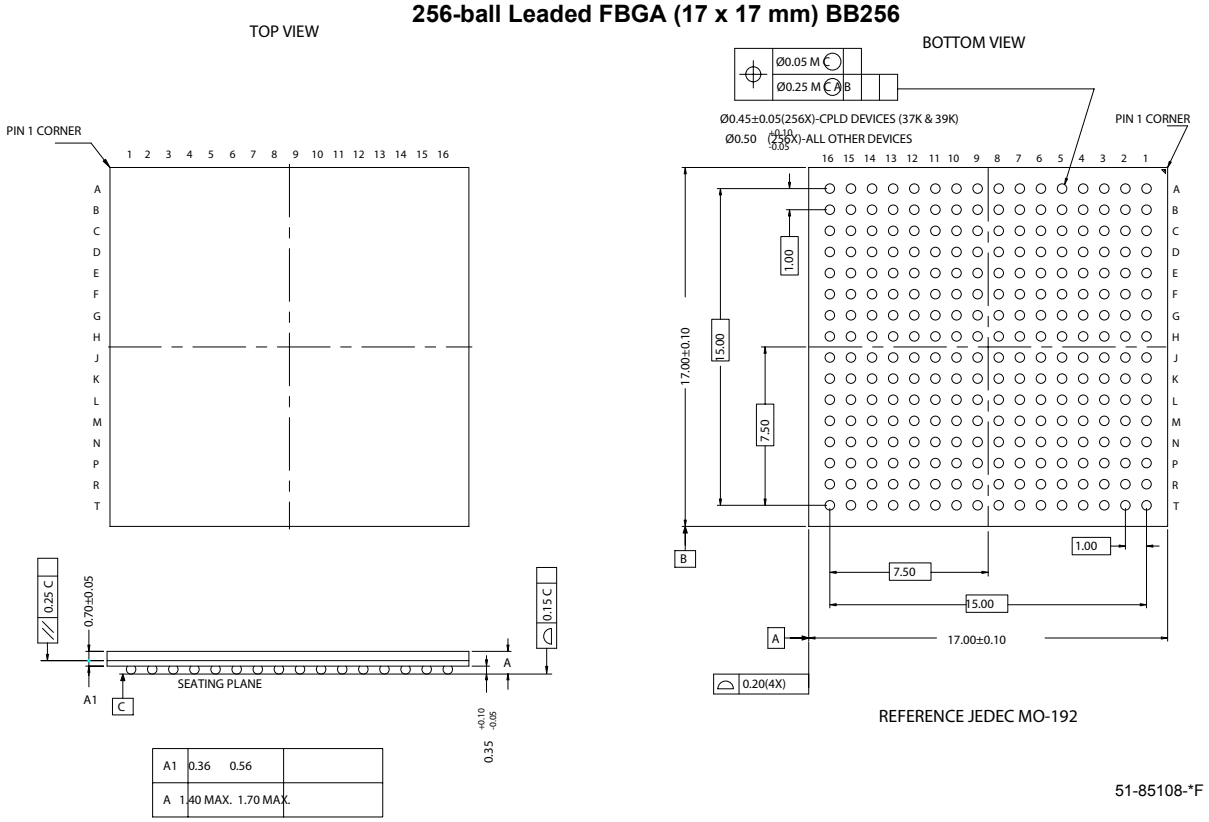
Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD09S18V18-200BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S18V18-200BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD09S18V18-167BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD09S18V18-167BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD09S18V18-167BBXI	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD09S18V18-167BBI	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Industrial

256K × 18 × 2 (4 Mbit) 1.8V/1.5V Synchronous CYDD04S18V18 Dual-Port SRAM (DDR only I/O)

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYDD04S18V18-200BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S18V18-200BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
167	CYDD04S18V18-167BBXC	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Commercial
	CYDD04S18V18-167BBC	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Commercial
	CYDD04S18V18-167BBXI	BW256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Lead-Free)	Industrial
	CYDD04S18V18-167BBI	BB256E	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Leaded)	Industrial

Package Diagrams

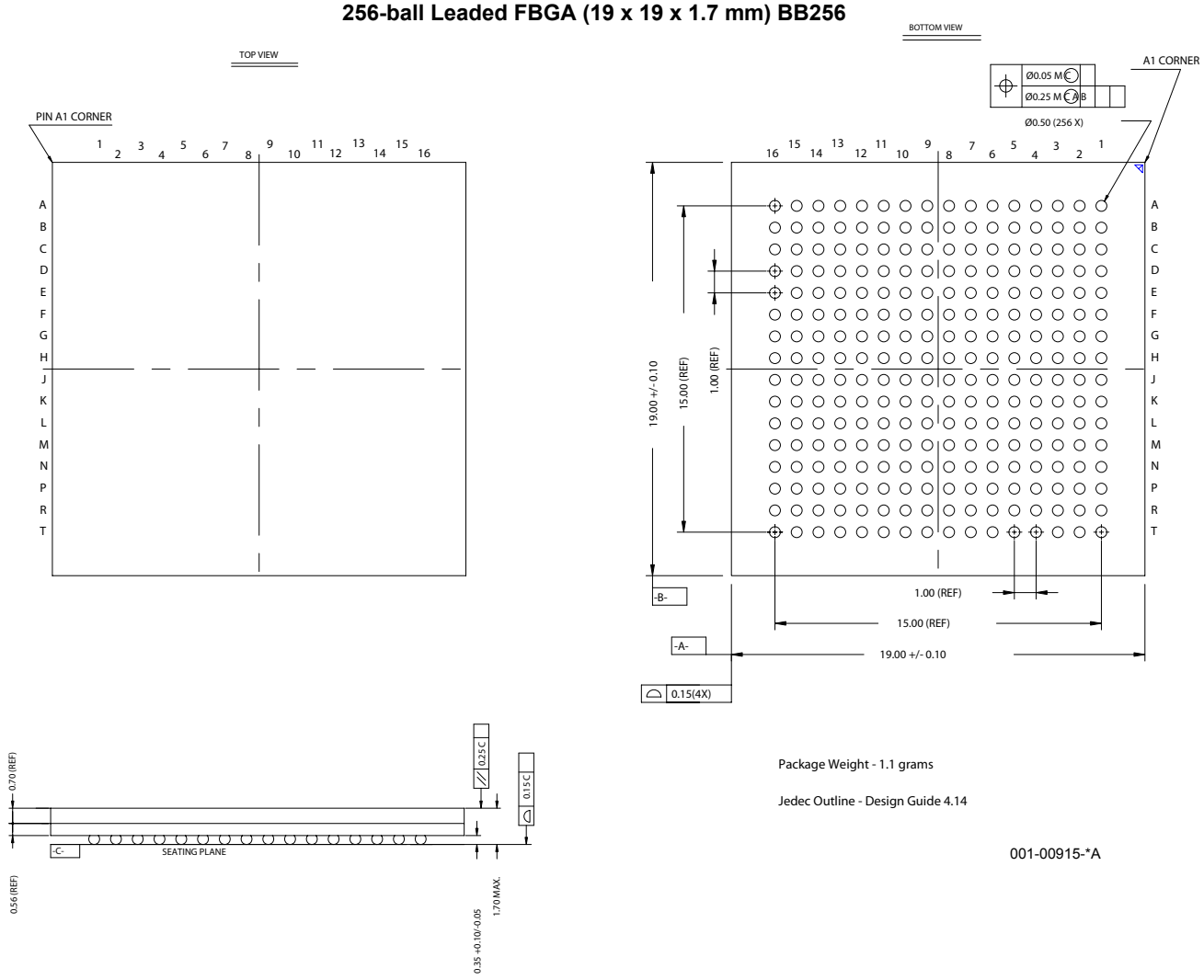
256-ball Lead-Free FBGA (17 x 17 mm) BW256
256-ball Leaded FBGA (17 x 17 mm) BB256



Package Diagrams (continued)

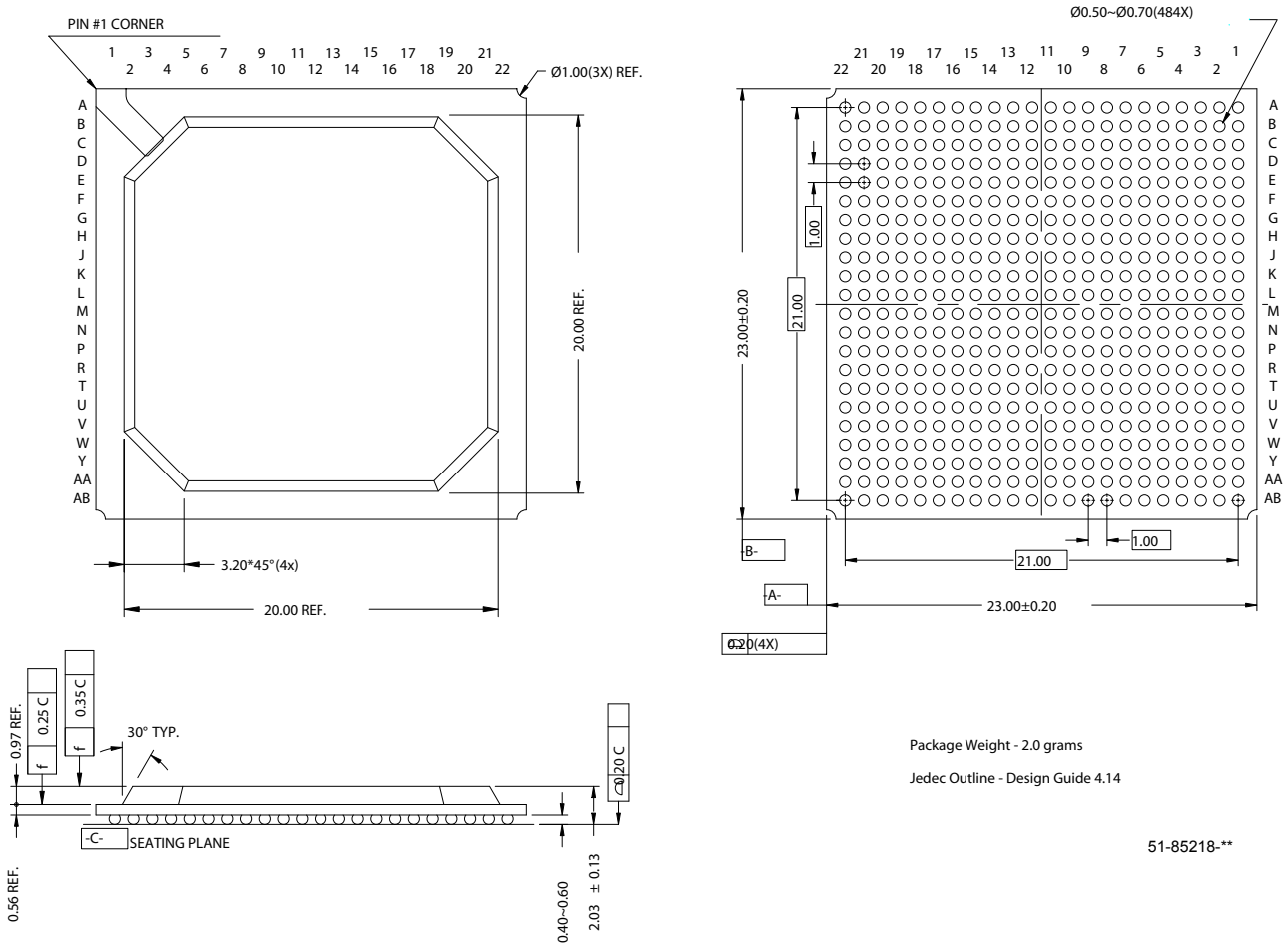
256-ball Lead-Free FBGA (19 x 19 x 1.7 mm) BW256

256-ball Leaded FBGA (19 x 19 x 1.7 mm) BB256



Package Diagrams (continued)

484-ball Lead-Free PBGA (23 mm x 23 mm x 2.03 mm) BY484
484-ball Leaded PBGA (23 mm x 23 mm x 2.03 mm) BG484



Package Weight - 2.0 grams

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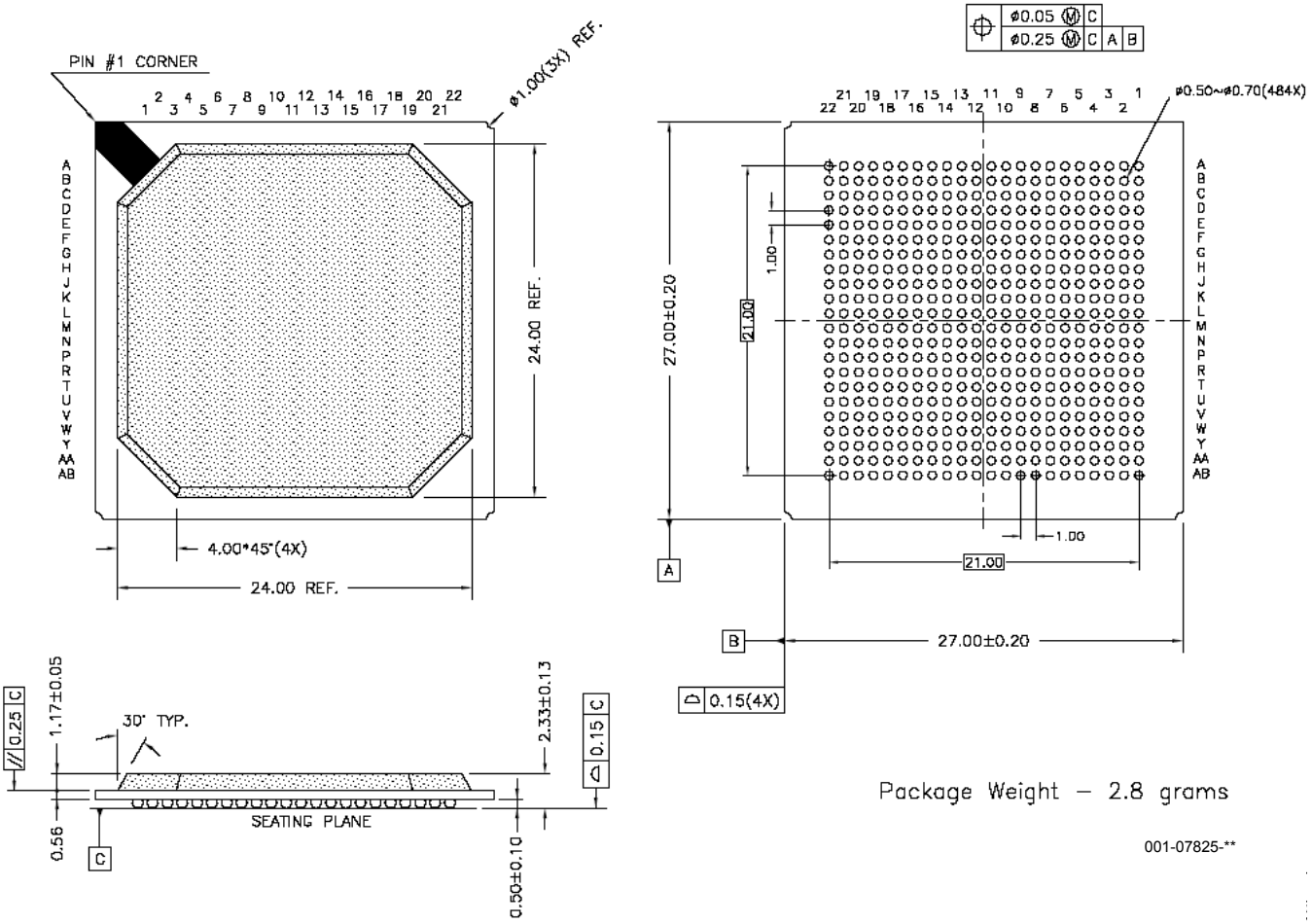
Package Diagrams (continued)

484-ball Lead-Free PBGA (27 mm x 27 mm x 2.33 mm) BY484S
484-ball Leaded PBGA (27 mm x 27 mm x 2.33 mm) BG484S



Document History Page

Document Title: FullFlex™ Synchronous DDR Dual-Port SRAM Document Number: 38-06072				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	274729	See ECN	SPN	New data sheet
*A	294239	See ECN	SPN	Updated VIM section Added notes 7 Added timing for 100 MHz with DLL Disabled Removed t_{PS}
*B	301331	See ECN	SPN	Added note 19 Updates Selectable I/O Standard Section
*C	318834	See ECN	SPN	Updated Block Diagram Updated 484 pinouts, changed pins D11, W12, K3, K20 Added note 4 - Leaving pin DNU disables VIM Updated 256 pinout, changed pins C10, G5, N7, N10 Added note 18, 19, 20, 21 Updated parameters in table 16 Updated note 1
*D	386692	See ECN	SPN	Updated ordering information Added statement about no echo clocks for flow-through mode Updated electrical characteristics Added note 27 (timing for x18 devices) Updated address readback latency to 2 cycles for DDR mode Updated DDR timing numbers for t_{CD}, t_{DC}, t_{CCQ}, t_{CQHQV}, t_{CQHQX}, t_{CKHZ}, t_{CKLZ} Updated input edge rate Removed -133 speed bin electrical characteristics and timing columns Updated Table 5 on collision detection to be the same as the one found in the EROS Added description of busy readback in collision detection section Changed dummy write descriptions Updated PORTSTD[1:0] connection details Updated ZQ pins connection details Updated address count notes Updated note 17, BO to BEO Added power supply requirements to $\overline{MRST}$ and VC_SEL Updated 484 ball package Changed name from FLEX72-E, FLEX36-E, AND FLEX18-E to FullFlex72, FullFlex36, and FullFlex18
*E	401662	See ECN	KGH	Updated $\overline{READY}$ description to include Wired OR note Updated master reset to include wired OR note for $\overline{READY}$ Updated electrical characteristics to include I_{OH} and I_{OL} values Updated electrical characteristics to include $\overline{READY}$ Added I_{IX3} Updated maximum input capacitance Added note 29 Updated Pin Definitions for CQ0, $\overline{CQ0}$, CQ1, and $\overline{CQ1}$ Changed voltage name from VDDQ to VDDIO Changed voltage name from V_{DD} to V_{CORE} Updated the Package Type for the CYDXXS36V18 parts Updated the Package Type for the CYDXXS18V18 parts Included the Package Diagram for the 256-Ball FBGA (19 x 19 mm) BW256 Included an OE Controlled Write for Flow-through Mode Switching Waveform Included a Read with Echo Clock Switching Waveform Included a Unit column for Table 5 Removed Switching Characteristic t_{CA} from chart Included t_{OHZ} in Switching Waveform $\overline{OE}$ Controlled Write for Pipelined Mode Included t_{CKLZ2} in Waveform Read-to-Write-to-Read for Flow-through Mode Updated AC Test Load and Waveforms Included FullFlex36 DDR 484-ball BGA Pinout (Top View) Included FullFlex18 DDR 484-ball BGA Pinout (Top View) Included Timing Parameter t_{CORDY}

Document Title: FullFlex™ Synchronous DDR Dual-Port SRAM Document Number: 38-06072				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*F	458129	SEE ECN	YDT	Changed ordering information with lead-free part numbers Removed VC_SEL Added I/O and core voltage adders Removed references to bin drop for LVTTL/2.5V LVCMOS and 1.5V core modes Updated Cin and Cout Updated ICC, ISB1, ISB2 and ISB3 tables Updated device widths information on first page Updated busy address read back timing diagram Added HTSL input waveform Removed HSTL (AC) from DC tables Added 484-ball 27mmx27mmx2.33mm PBGA package
*G	470037	SEE ECN	YDT	Changed VOL of 1.8V LVCMOS to 0.45V and VOH to VDDIO - 0.45V Updated tRSF VREF is left DNU when HSTL is not used Changed LVTTL/LVCMOS adder for DDR Formatted pin description table Changed VDDIO pins for 36Mx36 and 36Mx18 Changed 36Mx72 JTAG IDCODE
*H	499993	SEE ECN	YDT	DLL Change, added Clock Input Cycle to Cycle Jitter Modified DLL description Changed Input Capaciance Table Changed tCCS number Added note 34
*I	627539	SEE ECN	QSL	change all NC to DNU corrected switching waveform for (CQEN = High) from both Pipeline and Flowthrough mode to only pipeline mode Added note 17 to DDRON restriction Modified Master Reset Description Created a new table for flow-through mode only changed note 29 description Modified tSD, tHD, tSBE, tHBE, tCD, tDC, tCCQ, tCQHQV, tCQHQX, tCKHZ, and tCKLZ timing parameter Removed all instances of CYDD36S72V18